User's Guide

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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2411C Analysis Probe for Intel 80486DX/2/4/Overdrive, 80486SX/SL, and 80487SX

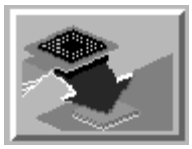
The HP E2411C Analysis Probe — At a Glance

The HP E2411C Analysis Probe provides a complete interface for state or timing analysis between any of the supported 80486/7 microprocessors listed below and HP logic analyzers. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

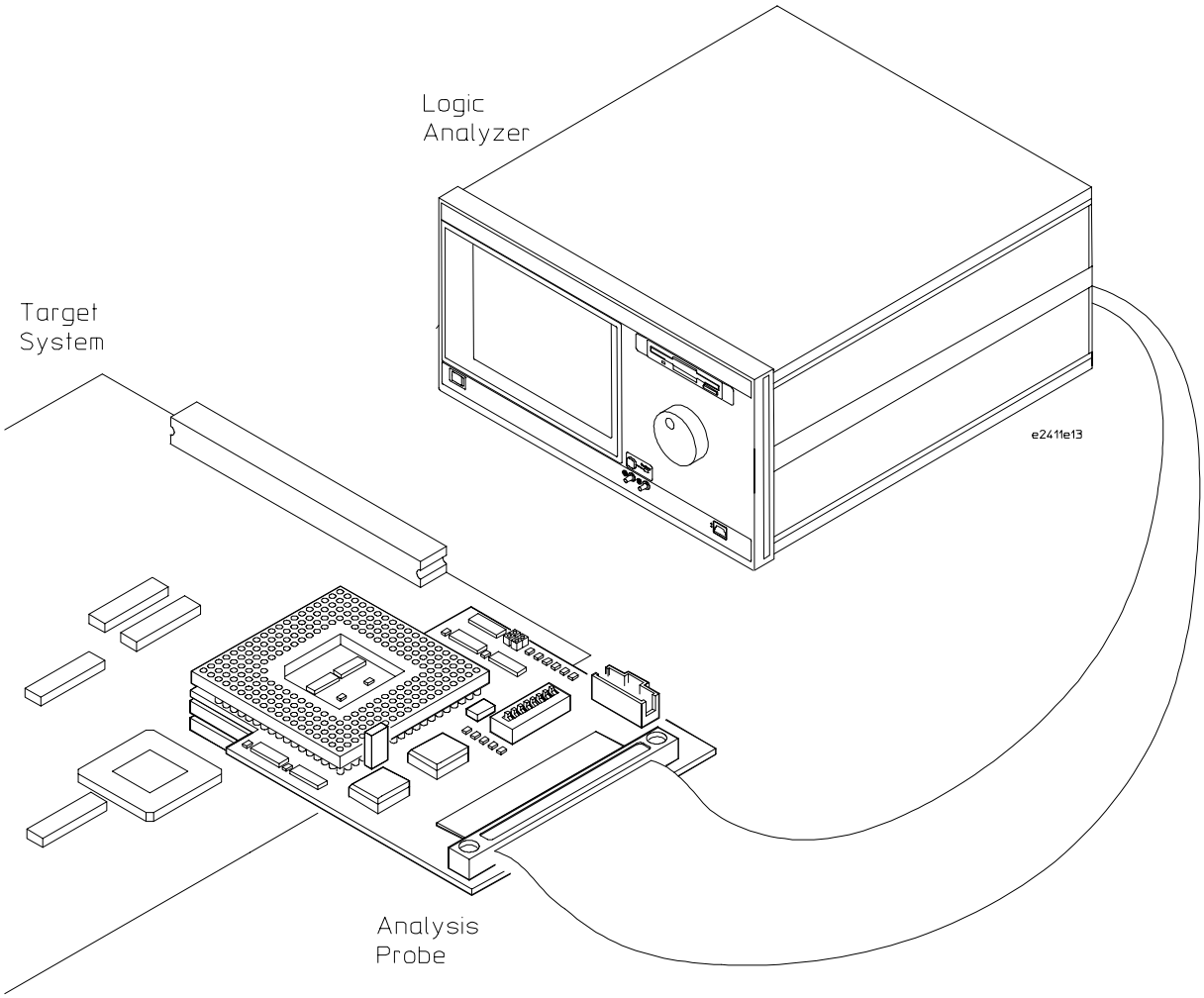
Microprocessor	Package	Ordering Information
80486DX2 Overdrive	236-, 237-, 238-, and 239-pin PGA	E2411C
80486DX/DX2/DX4	168-pin PGA	E2411C
80486SX	168-pin PGA	E2411C
80487SX	169-pin PGA	E2411C
80486SX	176-pin TQFP	E2411C and E5353A
80486SL	208-pin PQFP	E2411C, E5344A, and E5318A

The analysis probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software on the enclosed disks set up the logic analyzer for compatibility with the analysis probe. The inverse assemblers on the disks provide displays of the 80486/7 data bus in 80486/7 assembly language mnemonics.



If you are using the analysis probe with the HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference. The HP 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.

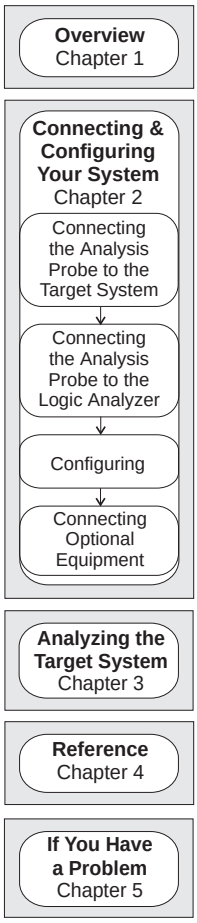


Analyzing a Target System with the HP E2411C Analysis Probe

In This Book

This book is the User's Guide for the HP E2411C Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

HP 16600 and HP 16700 Series Logic Analysis Systems

If you are using the analysis probe with HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The HP 16600 and HP 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

contents

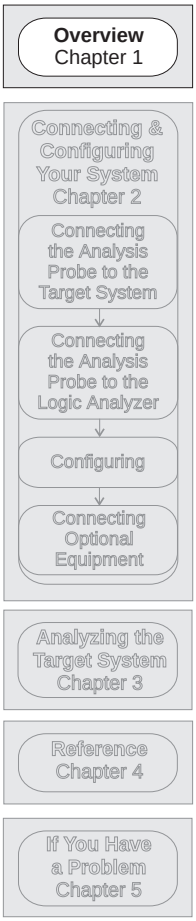
1

Overview

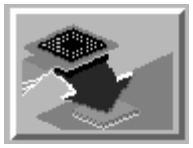
Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the HP 16600 and HP 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your HP 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the I80486 Processor Support Package. Use the procedure on the CD-ROM jacket to install the I80486 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the HP E2411C analysis probe. Logic analyzer software version requirements are shown on the following page.

The HP E2411C requires six logic analyzer pods (102 channels) for inverse assembly. The analysis probe contains one additional pod that you can monitor.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16550A (one or two cards)	102/card	100 MHz	250 MHz	4 k states
16554A (two cards)	68/card	70 MHz	125 MHz	512 k states
16555A (two cards)	68/card	110 MHz	250 MHz	1 M states
16555D (two cards)	68/card	110 MHz	250 MHz	2 M states
16556A (two cards)	68/card	100 MHz	200 MHz	1 M states
16556D (two cards)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the HP E2411C. You can obtain the latest software at the following web site:

www.hp.com/go/logicanalyzer

If your software version is older than those listed, load new system software with the above version numbers or higher before loading the HP E2411C software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with HP E2411C
HP 16600 Series	The latest HP 16600 logic analyzer software version is on the CD ROM shipped with this product.
HP 1660A/AS Series	A.03.01
HP 1660C/CS/CP Series	A.02.01
HP 1670A/D Series	A.02.01
Mainframes*	
HP 16700 Series	The latest HP 16700 logic analyzer software version is on the CD ROM shipped with this product.
HP 16500C Mainframe**	A.01.05
HP 16500B Mainframe**	A.03.14

* The mainframes are used with the HP 16550 and HP 16554/55/56 logic analyzer modules.
** The HP 16505A provides a windowed user interface for the HP 16500B/C Logic Analysis System. Refer to the *HP 16505A Prototype Analyzer Installation Guide* for information on connecting the HP 16505A to the HP 16500B/C Logic Analysis System. The HP 16505A requires software version A.01.30 or higher.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

HP E2411C

- The analysis probe, which includes the analysis probe circuit card and cables.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD ROM.
- Two pin protectors/adapters (168-pin and 238-pin).
- This User's Guide.

HP E5344A and HP E5318A (208-pin PQFP)

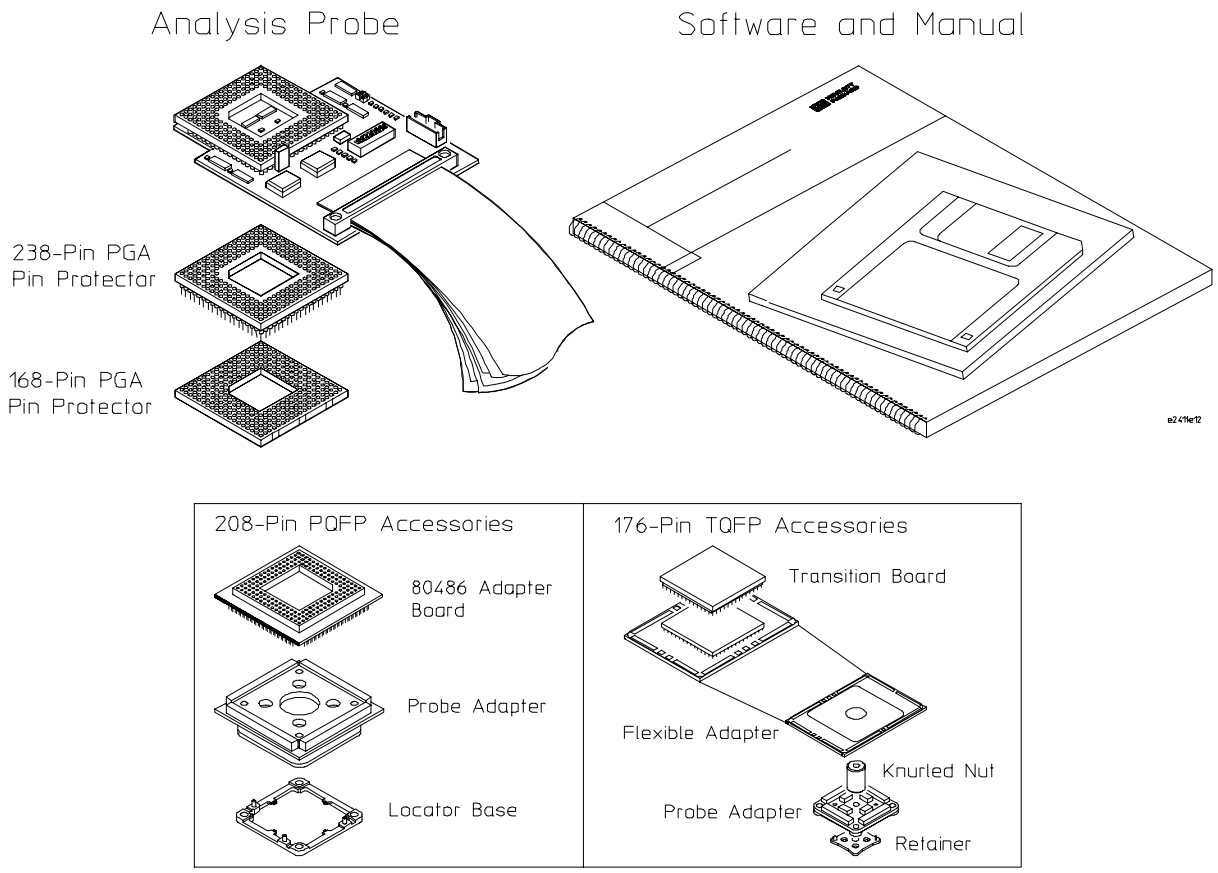
The 208-pin PQFP kit includes the following additional equipment:

- E5318A Probe Adapter, which includes an Installation Guide.
- E5344A 80486 Adapter Board.

HP E5353A (176-pin TQFP)

The 176-pin TQFP kit includes the following additional equipment:

- E5348A Elastomeric Probe Adapter, which includes an Installation Guide.
- E5350A General-Purpose Flexible Adapter.
- E5352A 80486 Transition Board.



Equipment Supplied with the HP E2411C

Minimum equipment required

For state and timing analysis of an 80486/7 target system, you need all of the following items.

- The HP E2411C Analysis Probe.
- For 208-pin PQFP target systems, the HP E5344A Locator Base Solution (Option 3).
- For 176-pin TQFP target systems, the HP E5353A Elastomeric Probing System (Option 4).
- For PQFP and TQFP target systems, sufficient area around the target system microprocessor (keep-out area) for the probe adapter. The keep-out areas are shown in the probe adapter installation guides.
- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

Additional equipment supported

Source-level Debuggers

The HP E2411C provides a connector for an Intel source-level debugger. The operating characteristics and pinout of the analysis probe debug port are listed in chapter 4.

You can obtain information on debuggers at the following web site:

www.hp.com/go/emulator

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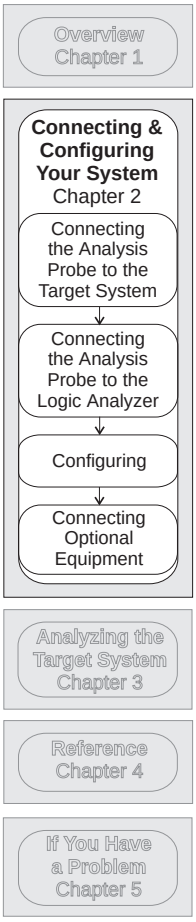
Connecting and Configuring Your System

Connecting and Configuring Your System

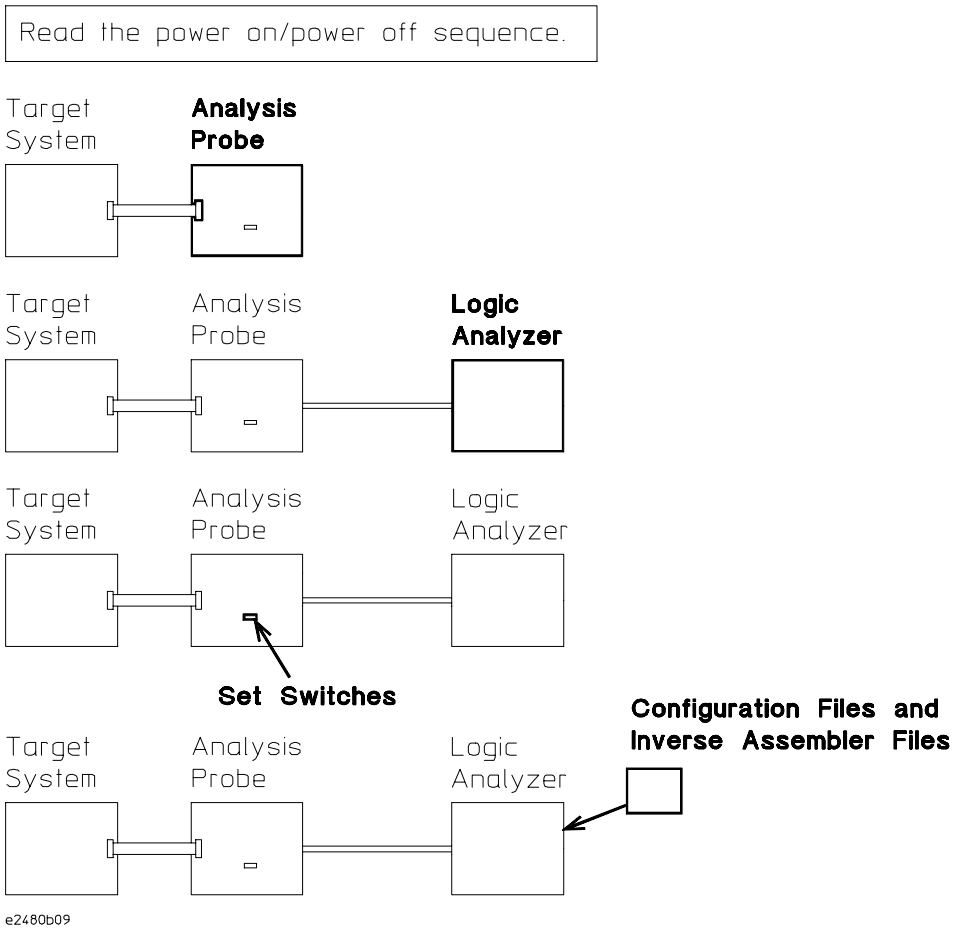


This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an HP 16600 or HP 16700 series logic analysis system, follow the instructions given on-screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment



Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on HP 16600 and HP 16700 series logic analysis systems

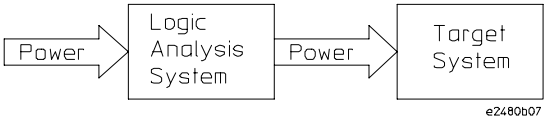
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

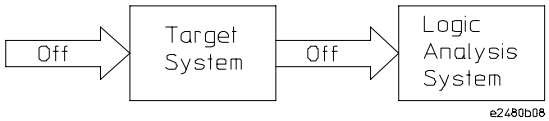
1. Logic analysis system.
2. Your target system.



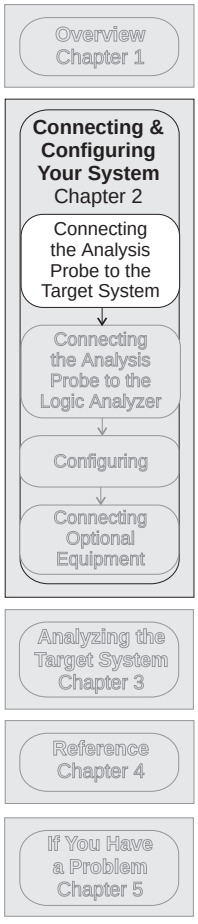
To power off

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.



Connecting the Analysis Probe to the Target System



This section explains how to connect the HP E2411C Analysis Probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- For PGA target systems, connect the analysis probe directly to the target system.

  Refer to "To connect to a PGA target system."

- For PQFP and TQFP target systems, connect the probe adapter to the target system.

  For PQFP target systems, refer to "To connect to a PQFP target system."

  For TQFP target systems, refer to "To connect to a TQFP target system."

- For PQFP and TQFP target systems, connect the analysis probe to the probe adapter.

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This protects the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins by covering them with the pin protector.

To connect to a PGA target system

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

1. Turn off the target system and disconnect all logic analyzer cables from the analysis probe.
2. Remove the 80486/7 microprocessor from its socket on the target system and store it in a protected environment.
3. For 80486DX2 Overdrive target systems, remove the 168-pin pin protector from the bottom side of the analysis probe PGA socket, and use only the 238-pin pin protector.
4. Prior to inserting the connector in the socket, note the position of pin A1 on the analysis probe connector and the target system socket (refer to the figure on next page).
5. Carefully align the analysis probe connector with the socket on the target system so that all pins are making contact.

CAUTION

Serious damage to the target system or analysis probe can result from incorrect connection. The pins on the HP E2411C are in the 238-pin Overdrive pattern. 80487SX users should note that there is an additional key at position E5. Chapter 4 contains pin diagrams.

6. Plug the analysis probe connector into the microprocessor socket on the target system.

   If the analysis probe circuit board interferes with components of the target system or if a higher profile is required, insert additional plastic pin protectors. You can order plastic pin protectors from Hewlett-Packard using the part number 1200-1790 (168-pin) or 1200-1789 (238-pin). However, any 168-pin or 238-pin PGA IC socket with an 80486 footprint and gold-plated pins can be used.

7. Plug the 80486/7 microprocessor into the socket of the analysis probe board.

   The socket on the analysis probe board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with a minimum amount of force.

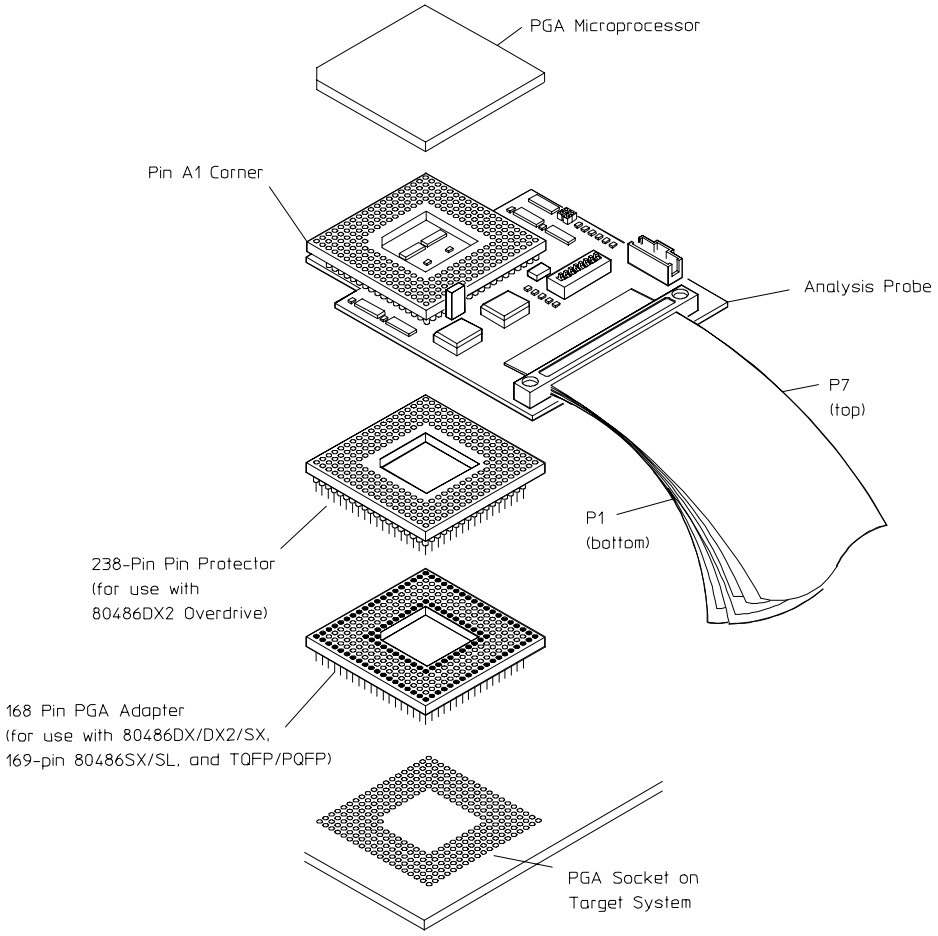
CAUTION

Do not use sharp objects or excessive force when removing a microprocessor or socket from the analysis probe board. Traces on the analysis probe board may be damaged.

CAUTION

Do not apply pressure to the PC board that will cause it to flex. This product has fine pitch PC traces and circuit mounted components. Flexing of the PC board places excessive force on the traces and components that could cause breakage of the traces, components, or solder joints.

When removing this product from the PGA socket, apply pressure only to the PGA sockets.



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Pin A1 Location

To connect to a PQFP target system

The HP E5344A Locator Base Solution provides a connection between the analysis probe and the Intel 208-pin 80486SL PQFP microprocessor. The probe adapter attaches over the microprocessor. A PGA transition socket allows the analysis probe PGA pins to connect to the probe adapter. The HP E5344A consists of the following:

- E5318A Probe Adapter, which includes an Installation Guide.
- E5344A 80486 Adapter Board.

The keep-out area showing the required clearances for the PQFP adapter are in the PQFP Probe Adapter Installation Guide.

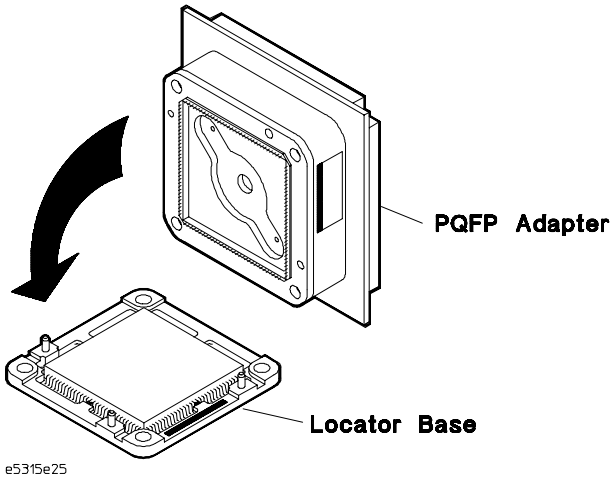
Use the following procedure to install the Locator Base Solution.

1 Install the PQFP adapter assembly.

CAUTION

Serious damage can be done to the target system or analysis probe from incorrect connection. Note the position of pin 1 on the target system and Pin A1 on the analysis probe prior to making any connection. Also, take care to align the pins so that all pins are making contact.

Follow the instructions in the probe adapter Installation Guide to install the PQFP adapter assembly.



Installing the Adapter Assembly, as Shown in the Probe Adapter Installation Guide

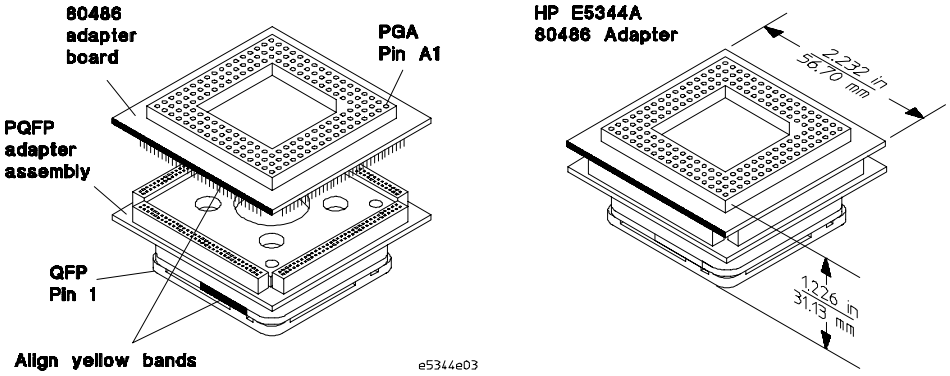
2 Attach the 80486 adapter board.

a Align the yellow band on your 80486 adapter board with the yellow band on the PQFP adapter assembly.

b Attach the adapter board to the adapter assembly by plugging it into the socket on top.

CAUTION

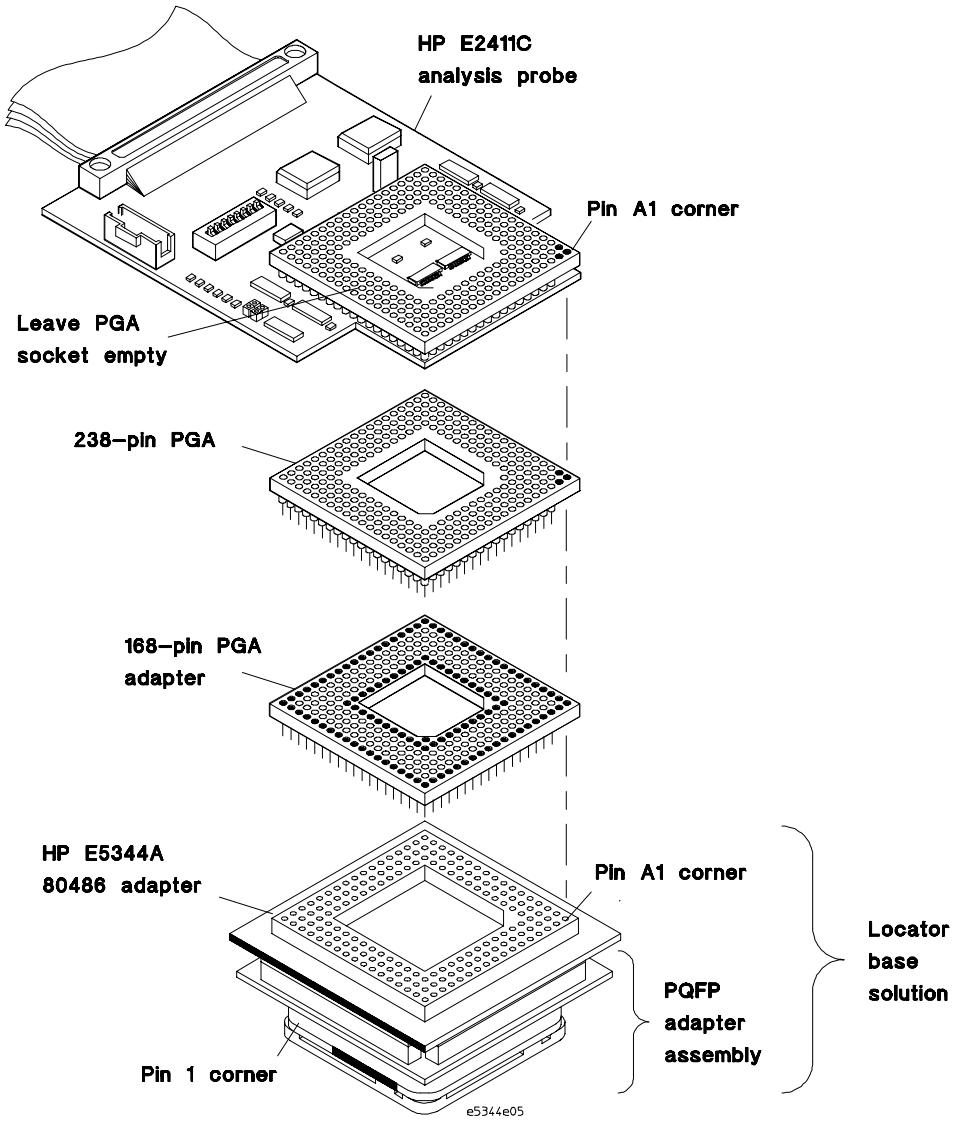
To prevent pin damage and ensure proper connection, make sure the adapter pins are aligned and seated correctly in the socket.



Installing the Adapter Board

3 Attach the HP E2411C analysis probe to the 80486 adapter (see figure next page).

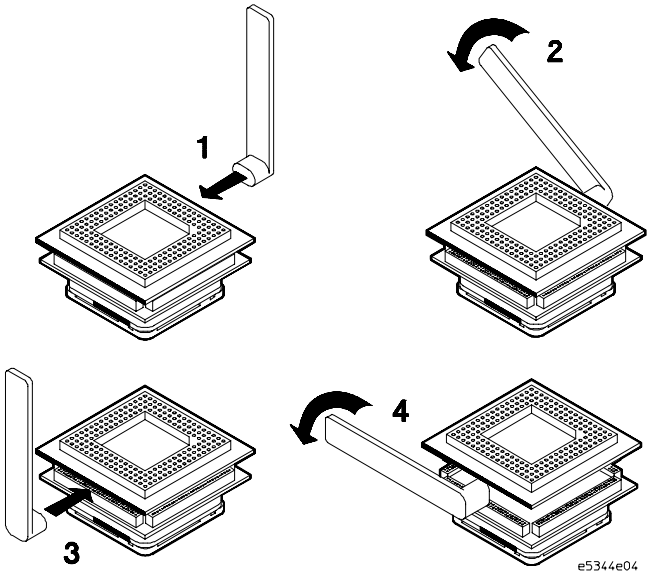
A PGA processor will not operate if plugged into the 80486 adapter board, or if plugged into the PGA socket on the analysis probe when the probe is connected to a PQFP target system. Leave the PGA socket of the analysis probe empty.



Connecting to a PQFP Target System

Removing the 80486 adapter board

- If you must remove the adapter board, gently pry the 80486 adapter board from the PQFP adapter assembly using the pry tool (HP P/N 5081-7784) as shown.



Removing the Adapter Board

To connect to a TQFP target system

The HP E5353A Elastomeric Probing System attaches to a 176-pin TQFP microprocessor, and provides a PGA socket for attaching the HP E2411C Analysis Probe. The HP E5353A consists of the following:

- E5348A Elastomeric Probe Adapter, which includes an Installation Guide
- E5350A General-Purpose Flexible Adapter
- E5352A 80486 Transition Board

The keep-out area showing the required clearances for the PQFP adapter are in the PQFP Probe Adapter Installation Guide.

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

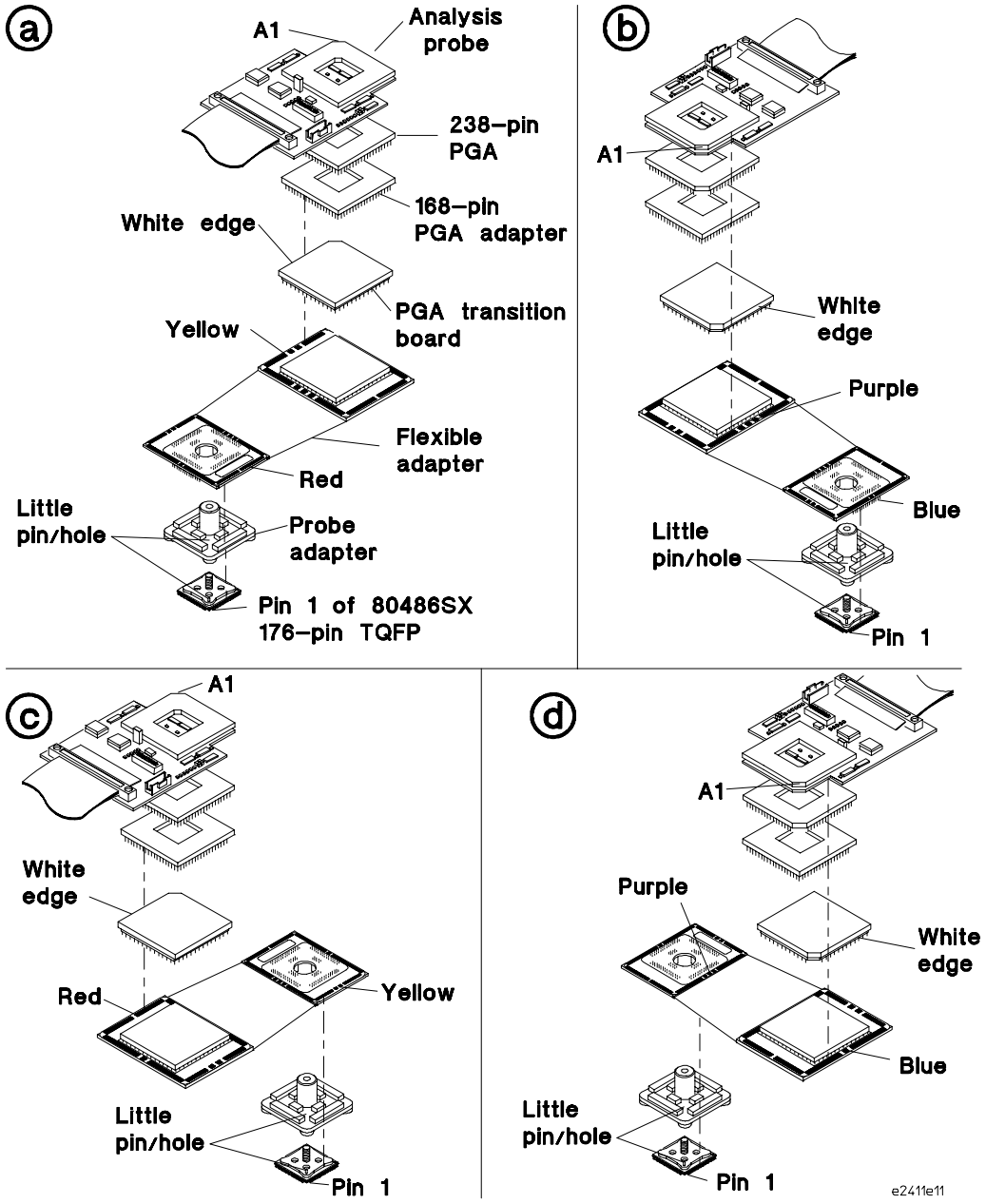
1. Turn off the target system and disconnect all logic analyzer cables from the analysis probe.
2. Select the rotation (shown on the next page) that best suits your target system. Note the following indicators on the illustration:
   - Position of Pin 1 on the microprocessor
   - Position of little pin on the retainer
   - Position of little hole on the probe adapter
   - Color code on both ends of the flexible adapter

     Note that the color selected on one end **will not match** the color selected on the other end.
   - Position of indicator on the transition socket
   - Position of Pin A1 on the analysis probe

   Flexible adapters can be installed in one of four rotations as shown in the illustration. This allows flexibility in attaching the analysis probe when target system components interfere.

CAUTION

Serious damage can be done to the target system or analysis probe from incorrect connection. Note the position of pin 1 on the target system and Pin A1 on the analysis probe prior to making any connection. Also, take care to align the pins so that all pins are making contact.



Rotations for HP E5353A Elastomeric Probing System and HP E2411C

3 Follow the instructions in the probe adapter Installation Guide to adhere the retainer and attach the probe adapter to the microprocessor.

4 Using the rotation selected in step 2 and the illustration on the previous page, attach the flexible adapter to the probe adapter.

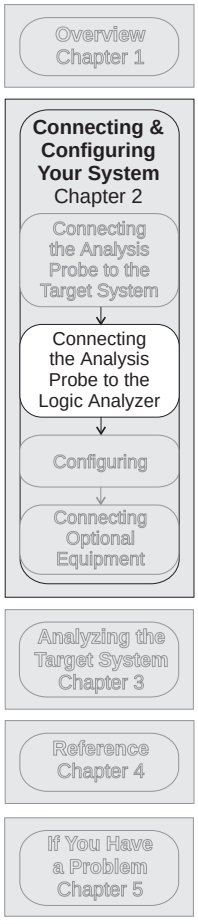
5 Using the rotation selected in step 2 and the illustration on the previous page, attach the transition board to the flexible adapter. The transition board has a white edge that aligns with a different color edge on the flexible adapter according to the rotation selected.

6 Using the rotation selected in step 2 and the illustration on the previous page, attach the PGA socket on the analysis probe to the transition board.

CAUTION

Serious Equipment Damage
Ensure that the analysis probe, pin adapters, transition board, flexible adapter, and probe adapter are aligned and seated correctly in the sockets. Serious equipment damage can result from incorrect connection. The final connection must match the rotation selected from the previous page.

Connecting the Analysis Probe to the Logic Analyzer



The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

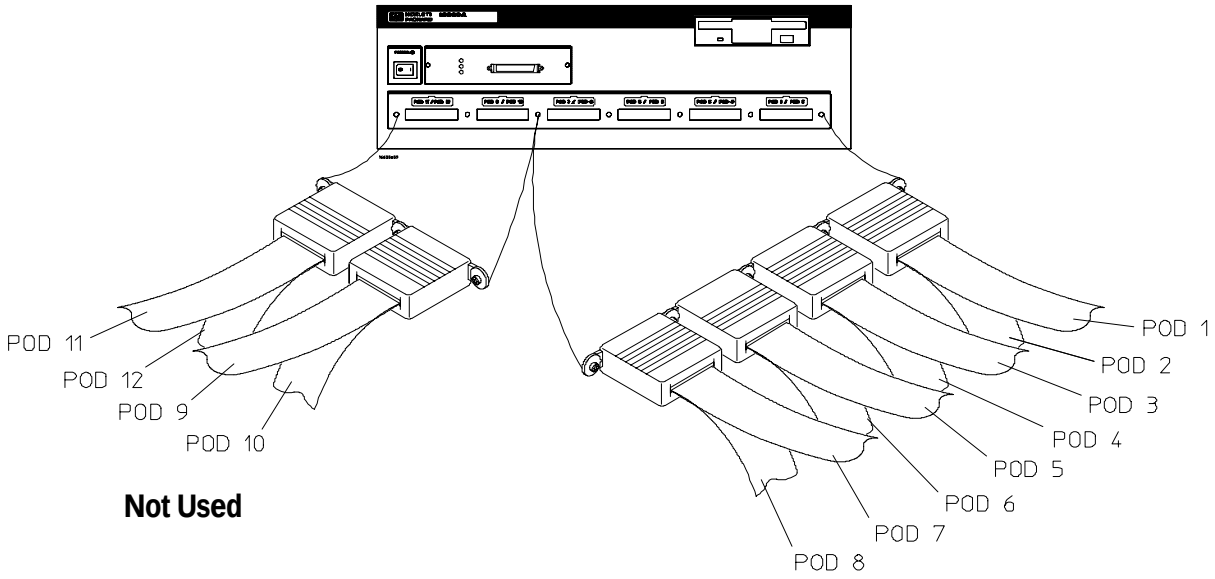
A minimum of six analysis probe pods are required for inverse assembly (P1, P2, P3, P4, P5, and P6). P7 contains signals which are primarily used on the 80486DX2 Overdrive microprocessor.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- HP 16600A logic analysis system
- HP 16601A logic analysis system
- HP 16602A logic analysis system
- HP 16550A logic analyzers (one or two cards)
- HP 16554/55/56 logic analyzers (two cards)
- HP 1660A/AS/C/CS/CP logic analyzers
- HP 1661A/AS/C/CS/CP logic analyzers
- HP 1670A/D logic analyzers
- HP 1671A/D logic analyzers

To connect to the HP 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16600A logic analysis system.

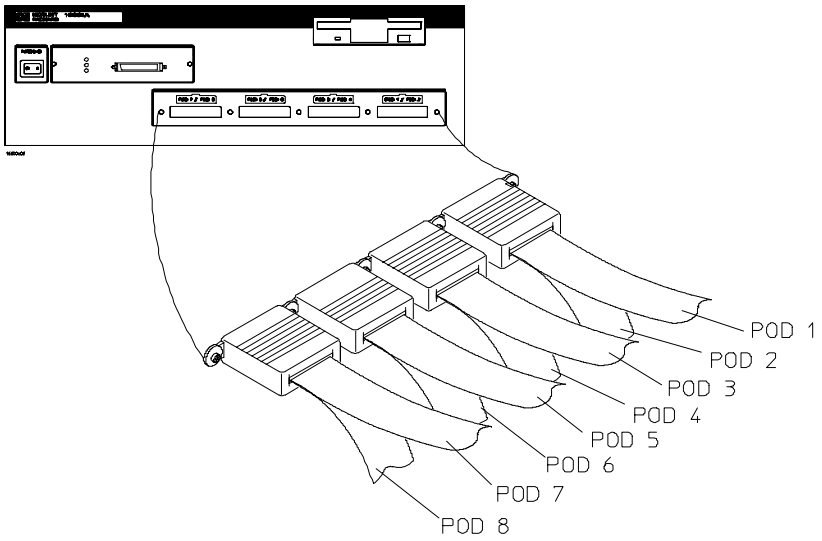


HP 16600	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2411C Connector	not used	P7 MISC	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S2 for the HP 16600 logic analysis system.

To connect to the HP 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16601A logic analysis system.

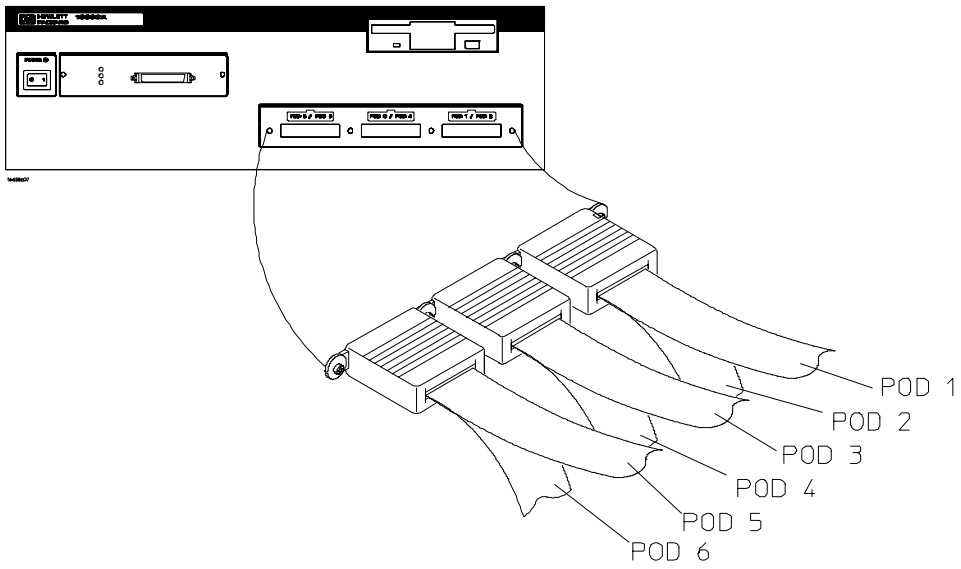


HP 16601	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2411C Connector	not used	P7 MISC	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S2 for the HP 16601 logic analysis system.

To connect to the HP 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16602A logic analysis system.

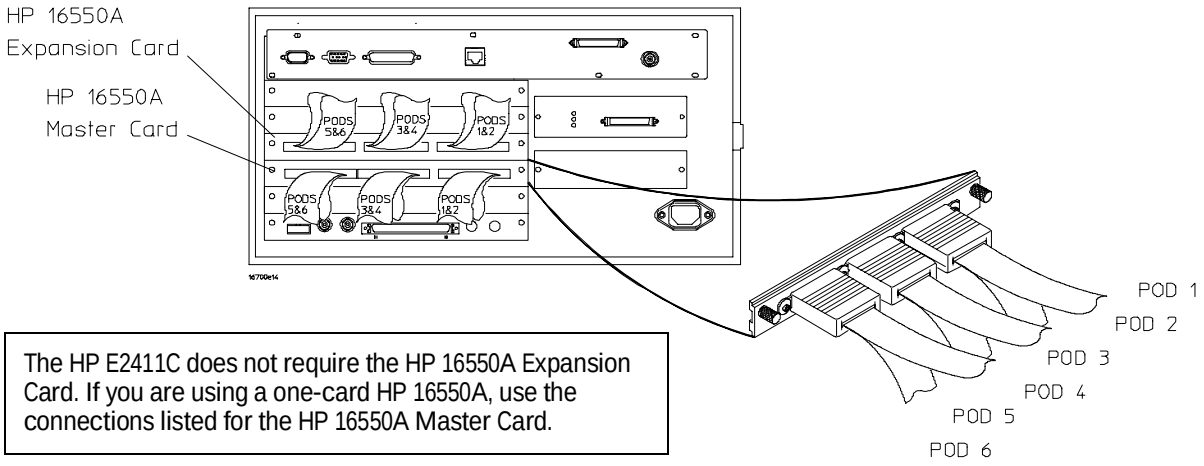


HP 16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2411C Connector	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S1 for the HP 16602 logic analysis system.

To connect to the HP 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the HP 16550A logic analyzer.



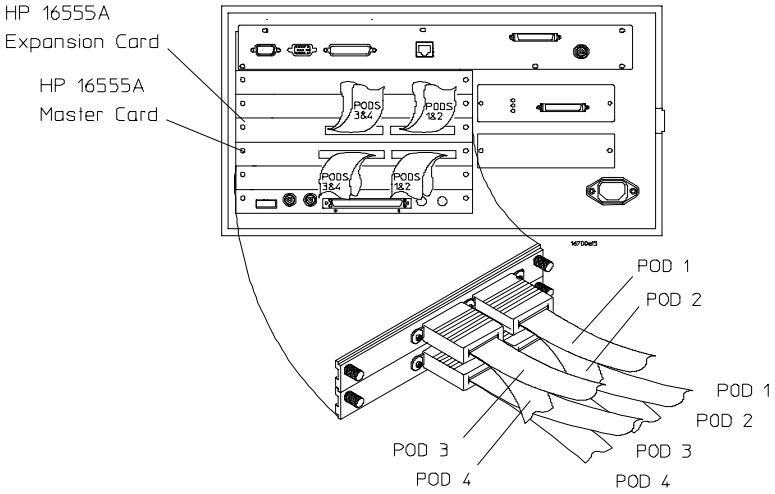
The HP E2411C does not require the HP 16550A Expansion Card. If you are using a one-card HP 16550A, use the connections listed for the HP 16550A Master Card.

HP 16550A Expansion Card	Expansion Card Pod 6	Expansion Card Pod 5	Expansion Card Pod 4	Expansion Card Pod 3	Expansion Card Pod 2	Expansion Card Pod 1
HP E2411C Connector	not used	not used	not used	not used	not used	P7 MISC
HP 16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2411C Connector	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S1 for the one-card HP 16550A logic analyzer and configuration file F486S2 for the two-card HP 16550A logic analyzer.

To connect to the HP 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the HP 16554A/55A/56A and HP 16555D/56D logic analyzers.

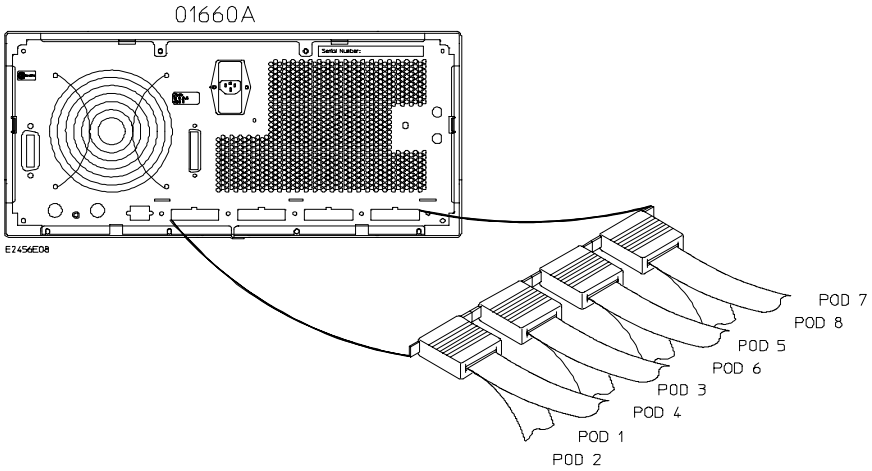


HP 16554/55/56 Exp. Card 1	Expansion Card 1 Pod 4	Expansion Card 1 Pod 3	Expansion Card 1 Pod 2	Expansion Card 1 Pod 1
HP E2411C Connector	not used	P7 MISC	P6 ADDR_H	P5 ADDR_L
HP 16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2411C Connector	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S2 for the HP 16554/55/56 logic analyzers.

To connect to the HP 1660A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1660A/C logic analyzers.

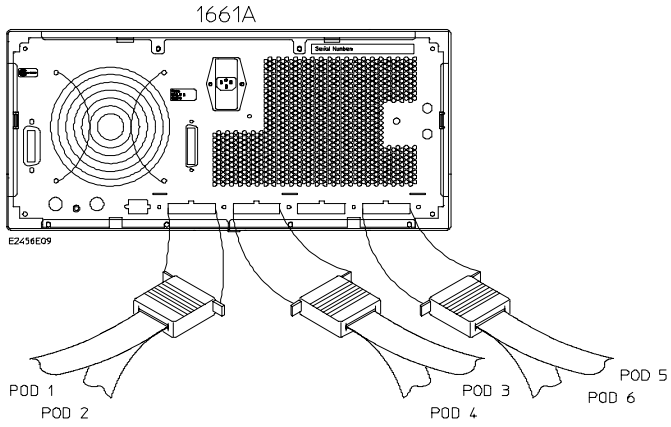


HP 1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6	Pod 7	Pod 8
HP E2411C Connector	P1 STAT_1 clk ↑	P2 STAT_2	P3 DATA_L	P4 DATA_H	P5 ADDR_L	P6 ADDR_H	P7 MISC	not used

Configuration File
Use configuration file F486S2 for the HP 1660A/AS/C/CS/CP logic analyzers.

To connect to the HP 1661A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers.

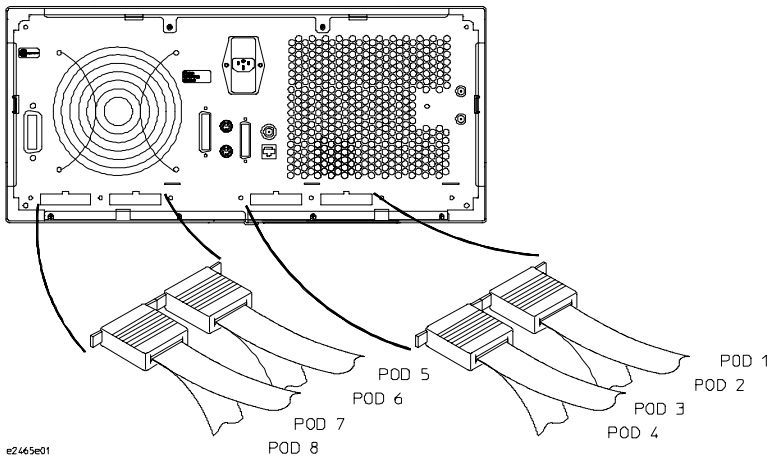


HP 1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
HP E2411C Connector	P1 STAT_1 clk ↑	P2 STAT_2	P3 DATA_L	P4 DATA_H	P5 ADDR_L	P6 ADDR_H

Configuration File
Use configuration file F486S1 for the HP 1661A/AS/C/CS/CP logic analyzers.

To connect to the HP 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1670A/D logic analyzers.

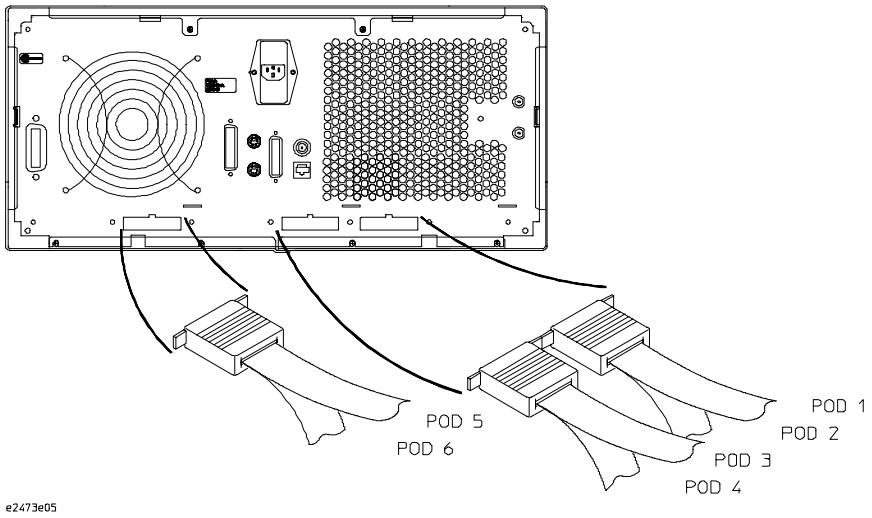


HP 1670A/D	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2411C Connector	not used	P7 MISC	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S2 for the HP 1670A/D logic analyzer.

To connect to the HP 1671A/D logic analyzer

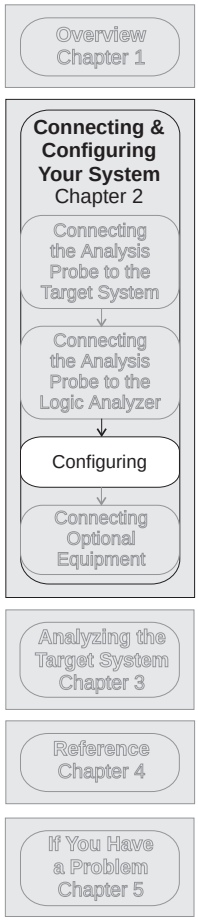
Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer.



HP 1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2411C Connector	P6 ADDR_H	P5 ADDR_L	P4 DATA_H	P3 DATA_L	P2 STAT_2	P1 STAT_1 clk ↑

Configuration File
Use configuration file F486S1 for the HP 1671A/D logic analyzer.

Configuring



This section shows you how to configure the HP E2411C Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe
- Configuring the logic analyzer

Configuring the Analysis Probe

Configuring the analysis probe consists of the following:

- Setting the State/Timing switch
- Setting the rest of the DIP switches

The State/Timing switch and the rest of the DIP switches are shown in the illustration on the following page.

To set the State/Timing switch

The analysis probe can operate in three modes: State-per-transfer, State-per-clock, or Timing. The State/Timing switch selects the mode. The LED on the analysis probe is amber for State and green for Timing.

1 For State-per-transfer or State-per-clock analysis, set the State/Timing switch to State.

In State mode, the active devices on the analysis probe latch and align the Address, Data, and Status bus. Inverse assembly is not available in State-Per-Clock mode. Note that you must go to the Format menu and change the clocking to switch between State-per-transfer and State-per-clock modes. See Chapter 3, "Modes of Operation" for additional information.

2 For Timing analysis, set the State/Timing switch to Timing.

In Timing mode, the active devices act as flow-through buffers. Inverse assembly is not available in Timing mode.

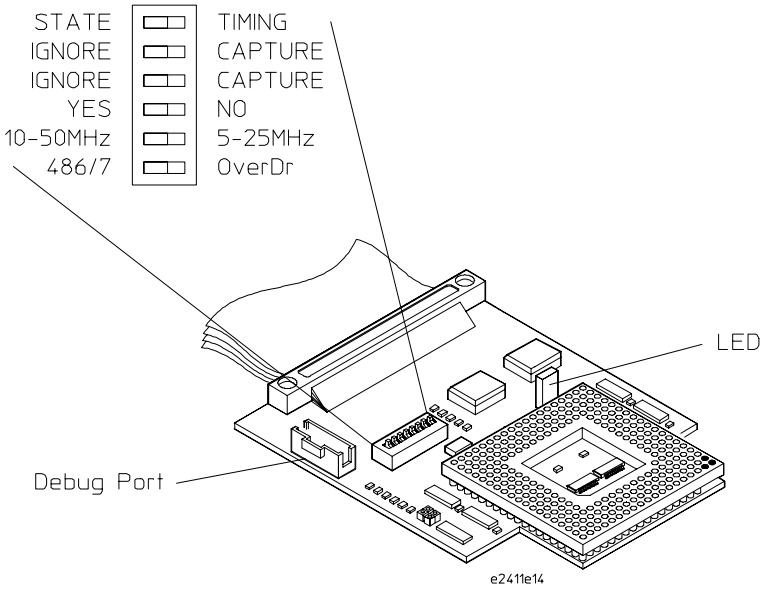
See Chapter 3, "Modes of Operation" for additional information on the operating modes.

To set the DIP switches

Six of the eight bits on the analysis probe DIP switch are used during operation (bits 0 - 5). Bits 0 - 3 affect the sampling, while bits 4 and 5 are configuration switches which must be set to match the microprocessor speed. The table below describes the effects of the switch settings.

Switch Settings

Switch Name	Down Position (Open)	Up Position (Close)
State/Timing	State	Timing
Cache Inv	Ignore	Capture
DMA	Ignore	Capture
DMA Tag	Yes	No
CLK Speed	10 - 50 MHz	5 - 25 MHz
Control	80486/7	Overdrive



DIP Switches, Including State/Timing Switch

Configuring the Logic Analysis System

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the HP 16600/700 series logic analysis systems, and another procedure for the HP 1660-series, HP 1670-series, and logic analyzer modules in an HP 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — HP 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/i80486/ exists.

> If the above directory does not exist, you need to install the I80486 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the I80486 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/i80486/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for 80486 analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an HP 1660-series, HP 1670-series, or logic analyzer modules in an HP 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 80486 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

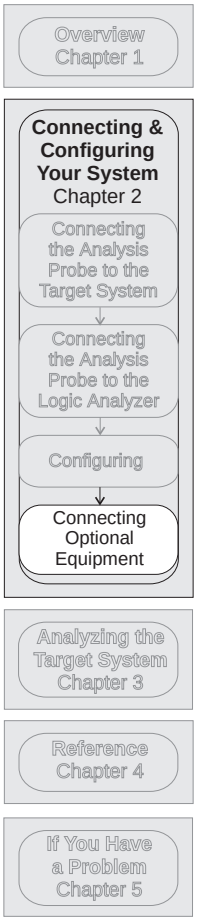
1. **Insert the floppy disk in the front disk drive of the logic analyzer.**
2. **Go to the Flexible Disk menu.**
3. **Configure the menu to load.**
4. **Use the knob to select the appropriate configuration file.**

   Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.
5. **Select the appropriate analyzer on the menu. The HP 16500 logic analyzers are shown in the Logic Analyzer Configuration Files table.**
6. **Execute the load operation on the menu to load the file into the logic analyzer.**

   The logic analyzer is configured for 80486 analysis by loading the appropriate configuration file. Loading this file also automatically loads an inverse assembler. There are two inverse assemblers, IA486 and IA486E. The configuration software checks the logic analyzer system during the load and automatically loads the appropriate inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File
16600A	na	F486S2
16601A	na	F486S2
16602A	na	F486S1
16550A (one card)	100 MHz STATE 500 MHz TIMING	F486S1
16550A (two card)	100 MHz STATE 500 MHz TIMING	F486S2
16554A (two card)	0.5M SAMPLE 70/125 MHz LA	F486S2
16555A (two card)	1.0M SAMPLE 110/250 MHz LA	F486S2
16555D (two card)	2.0M SAMPLE 110/250 MHz LA	F486S2
16556A (two card)	1.0M SAMPLE 100/200 MHz LA	F486S2
16556D (two card)	2.0M SAMPLE 100/200 MHz LA	F486S2
1660A/AS/C/CS	na	F486S2
1661A/AS/C/CS	na	F486S1
1670A/D	na	F486S2
1671A/D	na	F486S1



The remaining portion of this chapter describes additional equipment you can use. At the time this manual was printed, the following optional equipment was available for use with the analysis probe:

- Intel source-level debugger

Source-level Debuggers

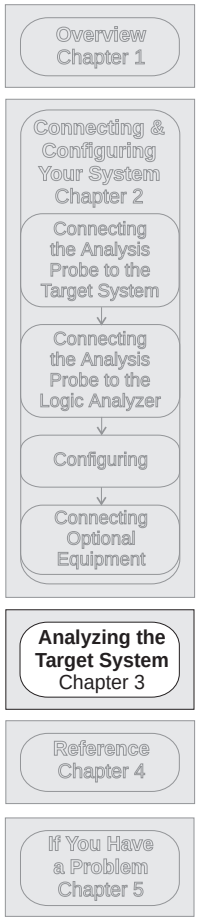
The HP E2411C provides a connector for an Intel source-level debugger. The operating characteristics of the analysis probe debug port are listed in chapter 4. Ensure that the power is removed from the target system and the logic analyzer before connecting a debugger to the debug port.

3

Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the HP E2411C analysis probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.



The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers
- Coprocessor support

Modes of Operation

The HP E2411C analysis probe provides three different analysis modes: State-per-transfer, State-per-clock, and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

In State-per-transfer mode, the analysis probe generates a K qualifier clock only when there is a valid data transfer. This allows the logic analyzer to capture only valid data when it appears on the bus. The inverse assembly software reconstructs the 80486/7 mnemonic from the hexadecimal data form. DMA and Cache Invalidation cycles may or may not be captured, depending on the settings of the respective switches. For State-per-transfer mode, the State/Timing switch must be set to "State." Inverse assembly is available in State-per-transfer mode.

State-per-clock mode

In State-per-clock mode, a state is captured on every rising edge of the microprocessor clock, regardless of the validity of the bus cycle. To use State-per-clock mode, change the clock in the Format menu from J rising edge with K qualifier high to J rising edge only. The Timing, Cache Invalidation, DMA, and DMA Tag switches have no effect on the data which is captured in State-per-clock mode. Inverse assembly is not supported in State-per-clock mode.

Timing mode

In Timing mode, the latches on the analysis probe act like flow-through buffers. The signals from the microprocessor go directly from the target system to the logic analyzer, with a 1-ns channel-to-channel skew. However, signals KEN#, BS8#, BS16#, and BOFF# are delayed by one clock.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trace specification

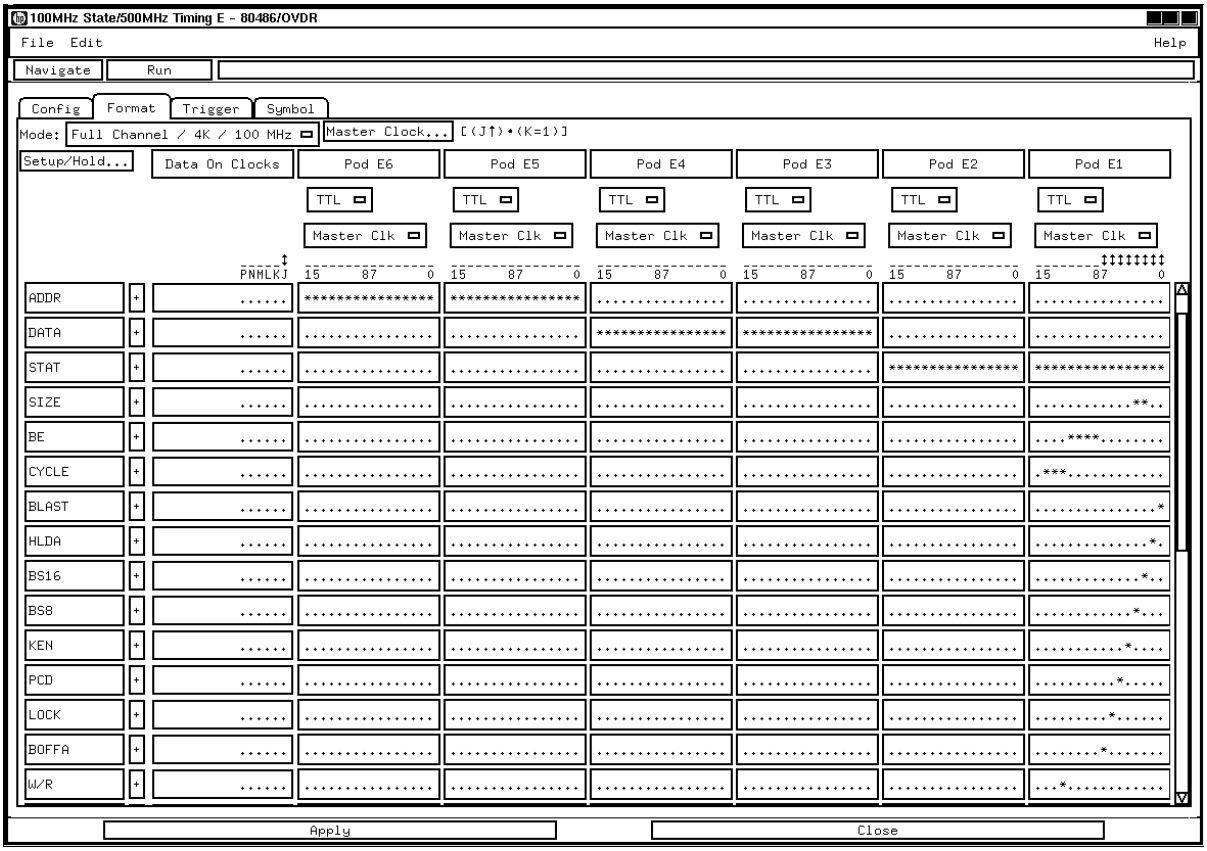
The trace specification is set up by the software to store all states. If you modify the trace specification to store only selected bus cycles, incorrect or incomplete disassembly may be displayed.

Format specification

The format specification set up by the software is configured for 3.5 ns setup/0 ns hold.

The configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor and any coprocessors connected directly to the microprocessor. The tables on the following pages show the signals used in the STAT label and the predefined symbols set up by the configuration files.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changing these labels may cause incorrect or incomplete inverse assembly.



Format Listing

Status Encoding

Each of the bits of the STAT label is described in the table below. Bit 0 is the least significant bit of the 32-bit field.

Only bits 0 - 15 are required for inverse assembly. Bits 16 - 31 are additional status bits which are available for logic analyzers which have more than 80 channels.

Status Label Bits

Bit	Status Signals	Description
0	BLAST#	The burst last signal indicates that the next time BRDY# is returned the burst bus cycle will be complete.
1	HLDA	The hold acknowledge signal indicates that the microprocessor has given the bus to another local master.
2	DBS16#	The bus size 16 signal is delayed one clock cycle because the microprocessor uses the value sampled at the clock before ready. The DBS16# signal indicates that the current transfer uses 16 bits of the data bus.
3	DBS8#	The bus size 8 signal is delayed one clock cycle because the microprocessor uses the value sampled at the clock before ready. The DBS8# signal indicates that the current transfer uses 8 bits of the data bus.
4	DKEN#	The cache enable signal (KEN#) is delayed one clock cycle because the microprocessor uses the value sampled at the clock before ready. The DKEN# signal is used to determine if the current cycle is cacheable.
5	PCD	The page cache disable signal.
6	LOCK#	The bus lock signal indicates that the current bus cycle is locked. The microprocessor does not allow a bus hold to occur when LOCK# is asserted.
7	BOFFA#	The backoff acknowledge signal is BOFF# delayed by one clock cycle. The bus is granted one clock after BOFF# is asserted.

Status Label Bits (Continued)

Bit	Status Signals	Description
8 - 11	BE0#-BE3#	The byte enable signals indicate which bytes are active during read and write cycles.
12	W/R#	The write/read signal is driven valid as the ADS# signal is asserted.
13	D/C#	The data/control signal is driven valid as the ADS# signal is asserted.
14	M/IO#	The memory/input-output signal is driven valid as the ADS# signal is asserted.
15	EADS#	The external address status signal indicates that a valid external address has been driven onto the microprocessor address pins. This address will be used to perform an internal cache invalidation cycle.
16	AHOLD	Asserting the AHOLD signal allows another bus master to access the address bus for a cache validation cycle.
17	INTR	The maskable interrupt signal indicates that an external interrupt signal has been generated.
18	RESET	The RESET input forces the 80486 to begin execution at a known state.
19	FLUSH#	The cache FLUSH input forces the 80486 to flush its entire internal cache.
20	BREQ	The BREQ signal indicates that the 80486 has generated a bus request.
21	HOLD	The HOLD signal indicates that another bus master has complete control of the bus. In response to HOLD, the 80486 will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles.

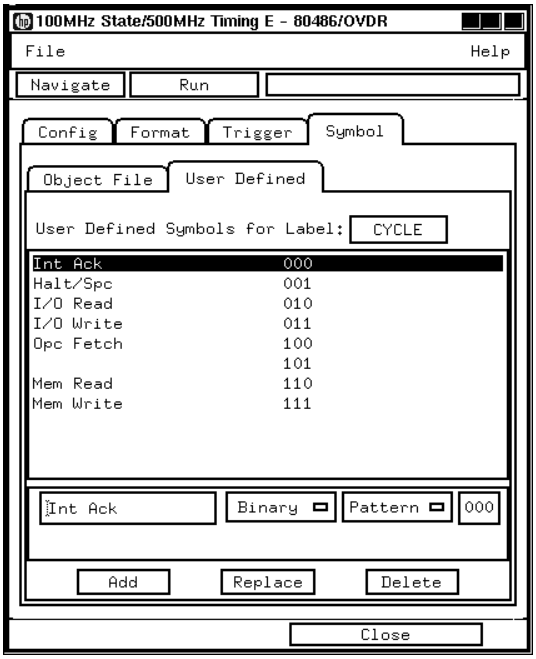
Status Label Bits (Continued)

Bit	Status Signals	Description
22	A20M#	When the Address Bit 20 Mask pin is asserted, the 80486 masks physical address 20 before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte which occurs on the 8086.
23	PLOCK#	The pseudo-lock signal indicates that the current bus transaction requires more than one bus cycle to complete.
24	PWT	The page write-through signal.
25	ADS#	The ADS# output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus.
26	RDY#	The non-burst ready signal indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the microprocessor in response to a write.
27	BRDY#	The burst ready input signal indicates that the external system has presented valid data in response to a read, or that the external system has accepted data in response to a write.

Logic Analyzer Symbols

The HP E2411C configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

The figure below shows the Int Ack symbols set up by the configuration software under the CYCLE label. The following table lists the rest of the labels and symbol encodings defined by the logic analyzer configuration software.



Symbols

Symbols

Label	Symbol	Pattern
CYCLE	INT ACK	000
	HALT/SPC	001
	I/O READ	010
	I/O WRITE	011
	OPC FETCH	100
	--	101
	MEM READ	110
	MEM WRITE	111
BE	BYTE 0	1110
	BYTE 1	1101
	BYTE 2	1011
	BYTE 3	0111
	LOW WORD	1100
	MIDDLE WORD	1001
	HIGH WORD	0011
	LOW 3 BYTES	1000
	HIGH 3 BYTES	0001
	DOUBLE WORD	0000
SIZE	8 BIT TRANSFER	0X
	16 BIT TRANSFER	10
	32 BIT TRANSFER	11
KEN	DISABLE CACHE	1
	ENABLE CACHE	0
HLDA	--	0
	486 IS OFF BUS	1
W/R	READ	0
	WRITE	1
D/C	CONTROL	0
	DATA	1
M/IO	I/O	0
	MEMORY	1
LOCK	--	1
	LOCKED CYCLE	0

Symbols (continued)

Label	Symbol	Pattern
PCD	--	0
	PAGE CACHE DISABL	1
PWT	--	0
	PAGE WRITE THRU	1
BRDY	INVAL BURST DATA	1
	VALID BURST DATA	0
RDY	INVALID DATA	1
	VALID DATA	0
BLAST	NOT LAST BUR CYC	1
	LAST CYC OF BURS	0
BOFFA	--	1
	BACKOFF ACK	0
ADS	INVALID ADDR	1
	VALID ADDR	0
EADS	--	1
	CI ADDR VALID	0
INTR	--	0
	INTR REQ	1
RESET	RESET	1
	RUN	0
FLUSH	--	1
	FLUSH CACHE	0
BREQ	--	0
	BUS REQ BY 486	1
HOLD	--	0
	DMA REQUESTED	1
A20M	--	1
	1 MB A WRAP REQ	0

The 80486 analysis probe contains two inverse assemblers, IA486 and IA486E. IA486E contains all the functions of the IA486 inverse assembler, plus additional features. For information on the IA486E features, see "The IA486E inverse assembler" on page 3-22.

The configuration software checks the logic analyzer during the load process. If the logic analyzer has the appropriate software version, the configuration file loads the enhanced inverse assembler. For information on the logic analyzer operating system version requirements, refer to "Logic analyzer software version requirements" on page 1-5.

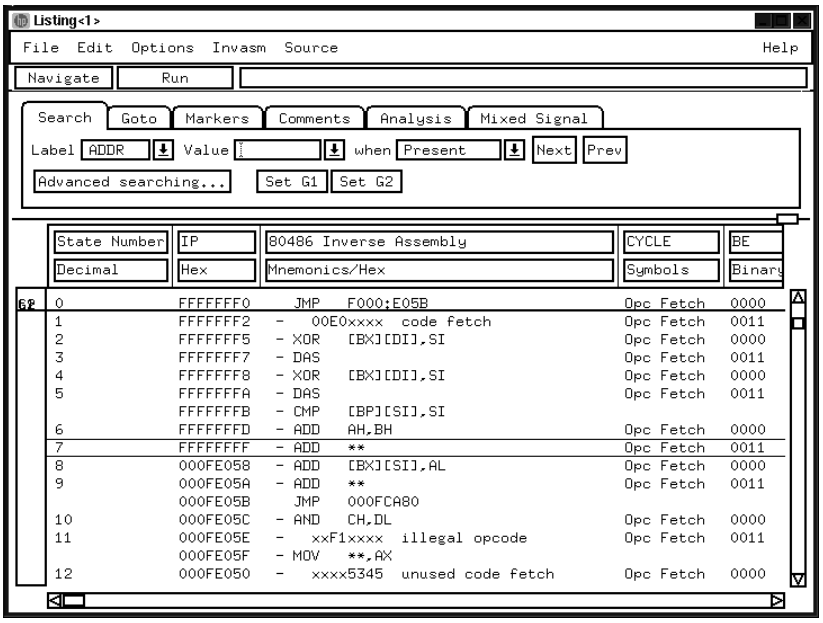
The following sections describe the features common to both inverse assemblers.

Listing menu

Captured data is displayed as shown below and on the next page. The second listing has unexecuted prefetches suppressed. These figures display the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly language source code.

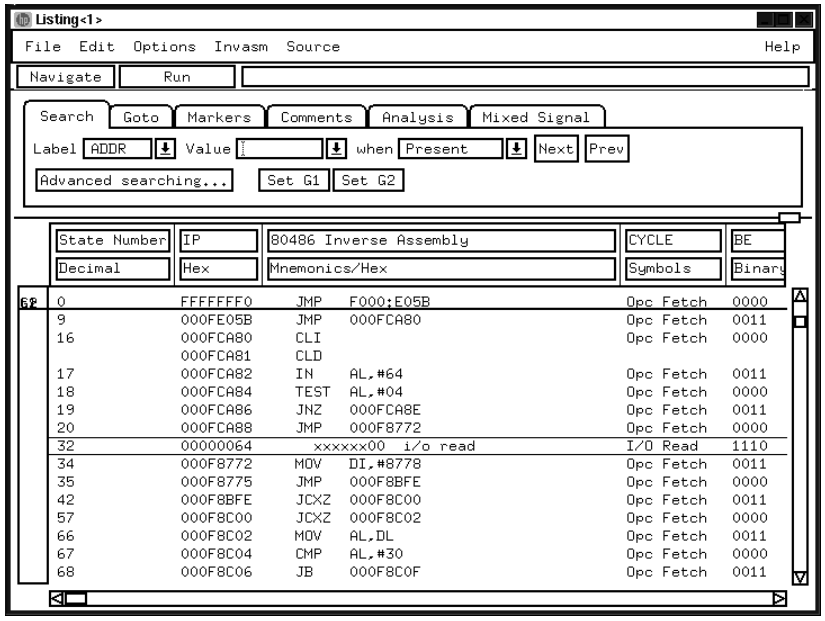
The logic analyzer always probes the full 32-bit data bus of the 80486. There are some memory systems that occasionally use only 8 or 16 bits for memory transactions. Some cycles transfer data on less than all four bytes of the data bus. This occurs with a combination of the byte enable signals from the microprocessor to memory and bus size signals (BS8# and BS16#) from memory to the microprocessor. When a memory cycle uses fewer than the full 32 bits of the data bus, the inverse assembler marks the bits not used by the microprocessor with an "x."

The "#" symbol in the state listing for the analysis probe refers to an immediate operand. A minus sign (-) indicates a prefetched instruction. Asterisks (**) indicate the logic analyzer did not obtain the data.



State Listing

The figure below shows the listing display with the IA486E inverse assembler. The unexecuted prefetches have been suppressed. A comparison of this figure and the one on the previous page shows the display filtering.



State Listing with Unexecuted Prefetches Suppressed

To align the inverse assemblers

The 80486 microprocessor fetches instructions 4 bytes (32 bits) wide at a time in a single bus cycle. However, the microprocessor does not indicate externally which of the bytes fetched is the first byte of an opcode fetch. You must "point" to the first byte of an opcode fetch. Once aligned, the inverse assembler disassembles from this state through the end of the display.

The 80486 microprocessor can execute the 80386 and 80486 instruction set (32-bit) or the object code from Intel's 16-bit microprocessor family, including software designed for Intel's 8086 and 80286. You must specify whether the code being executed was originally designed to run on Intel's 16 or 32-bit microprocessors when aligning the inverse assembler.

Use the following procedure to align the inverse assembler:

1. Select a line on the display that you know contains the first byte of an instruction fetch.
2. Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the State Listing with Unexecuted Prefetches Suppressed, line 0 is the top of the display.

3 Select the appropriate field for your analyzer or inverse assembler.

a For the HP 16600/700 series analyzers, select "Invasm," then select "Align." Two pop-up menus appear with the following choices:

```
0  1  2  3              SIZE 16
4  5  6  7
8  9  A  B
C  D  E  F
```

Size, as used here, refers to the default operand size for this code. This field toggles between 16 and 32.

b For the IA486E inverse assembler in other logic analyzers, select "Invasm Options" and use the "Code Synchronization" submenu. The same choices as above are available.

c For the IA486 inverse assembler, select the "Invasm" field at the top of the display. The following choices are available.

```
Size 16 Byte 0          Size 16 Byte 1
Size 16 Byte 2          Size 16 Byte 3
Size 32 Byte 0          Size 32 Byte 1
Size 32 Byte 2          Size 32 Byte 3
```

4 Select the choice that identifies which byte of the captured state contains the first byte of the code fetch and what the default operand size is for this code (16 or 32 bits).

5 Select "Align" to align the code.

The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 5.

Inverse assembler output format

The following paragraphs explain the operation of the inverse assemblers and the results you can expect in certain conditions.

Instruction Decoding

The analysis probe sends all of the microprocessor bus transactions to the logic analyzer. The time count accurately reflects when the end of the bus cycle occurred. Typically, several states separate the memory (or I/O) transfer from the instruction that caused the transfer.

State Data Format

The numeric output from the inverse assembler is in hexadecimal format; therefore, no base suffixing is incorporated.

The "#" symbol in the state listing for the analysis probe refers to an immediate operand. A minus sign (-) indicates a prefetched instruction. Asterisks (**) indicate the data was not obtained by the logic analyzer.

The 80486 can fetch a double word with four instruction bytes from program memory during a single read cycle. Therefor, up to four instructions may be displayed for a single analyzer state. If the least significant byte of this double word contains a single-byte instruction, the next sequential instruction begins in the next higher byte. This process continues from the least significant byte to the most significant byte until all of the bytes of the fetched double word are used. When a single state contains more than one instruction, each instruction is displayed on a separate line. For example:

```
+0015          =NEG    ECX                        OPCODE FETCH
               = MOV   BYTE PTR [EBP][-1B].CL
+0016          =  xxxxxxDA  mem read              MEMORY READ
```

Line number +0015 displays two instructions from a double word.

Because instructions may begin in any byte position, the last bytes of a multiple-byte instruction may extend into the lower bytes of the next double word fetched. In this instance, the next sequential instruction begins in the next higher byte of the next double word after the previous instruction and operands. When interpreting a given state, the inverse assembler ignores bytes used by a previous instruction and only displays the instructions that begin in that state. For example:

Byte Position				
3	**2**	**1**	**0**	
01	20	BB	90	Three-byte instruction MOV BX 0120H starts in byte 1.
10	BF	D2	31	Double-byte instruction XOR DX,DX (31D2) begins in byte 0. and continues into byte 1. Next instruction MOV DI, 0010H begins in byte 2, and continues into byte 0 of the next state.
F7	C8	8C	00	Single-byte instruction MOV AX,CS begins in byte 1. Double-byte instruction DIV DI (F7F7) starts in byte 3 and continues into byte 0 of next double word fetched.
30	CA	81	F7	Next instruction OR DX, # begins in byte 2 immediately after last instruction.

The inverse assembler output indicates that a portion (or portions) of an instruction is not captured by the analyzer by displaying "no operand" or "**." Missing operands occur and are primarily due to microprocessor prefetch activity. Storage qualification can also lead to such occurrences.

"="

The 80486 has two possible default operand/address sizes, 16 or 32 bits. This attribute is set when a code segment descriptor is loaded, and is impossible for the inverse assembler to detect. Therefore, you must manually declare the size by selecting the correct field under the Invasm pop-up menu. Any instruction with an operand size of 32 bits (either by default, or by using the operand override prefix) is marked with an "=" symbol in the third column of the 80486 mnemonic field to help you distinguish 32-bit operands from 16-bit operands.

Incorrect Disassembly

If the inverse assembler seems to be disassembling incorrectly by displaying registers such as "AX" and "EAX", it is likely that the size attribute is set incorrectly. Use the Invasm menu and select the appropriate register size.

The 80486 microprocessor can perform byte, word, and three-byte transfers, as well as double-word transfers between microprocessor registers and memory. Byte transfers can occur in any byte on the 32-bit data bus. Word and three-byte transfers can occur across any contiguous set of bytes that hold the transfer. The bytes that are valid in a transfer are indicated by the microprocessor BE0# through BE3# lines. The inverse assembler displays "xx" (don't care) for the bytes of a transfer that are ignored by the microprocessor. In this way it is possible to determine exactly which bytes were used by the microprocessor. For example:

xxxxxxDB	read memory	(Byte transfer on byte 0)
xxxx28xx	read memory	(Byte transfer on byte 1)
xxB3xxxx	read memory	(Byte transfer on byte 2)
ECxxxxxx	read memory	(Byte transfer on byte 3)
xxxx28DB	read memory	(Word transfer on lower word)
xxB328xx	read memory	(Word transfer on middle word)
ECB3xxxx	read memory	(Word transfer on upper word)
xxB328DB	read memory	(3-byte transfer on lower three bytes)
ECB328xx	read memory	(3-byte transfer on upper three bytes)
ECB328DB	read memory	(Double-word transfer)

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Because the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 32-bit intrasegment offset) is displayed instead of a mapped physical address.

Unexecuted Code Read Marking

The inverse assembler attempts to mark unexecuted code reads. Unexecuted code reads are the result of the interactions between the prefetch unit and program branches taken.

The unexecuted-prefetch mark (-) is found in the second column of the inverse assembly display, right after the byte address column. The "-" marking indicates that the branch was taken, and these instructions are indeed unexecuted. The inverse assembler does not always have enough information to determine if a conditional branch was taken; in those instances, it will assume that the branch was not taken.

Unexecuted code read markings help keep the inverse assembler synchronized because branch targets can often be located and identified as the starting byte of an instruction. There are cases, however, where the branch target byte address cannot be identified (the JMP reg command, for example), so re-synchronization may be necessary.

Branching to an Address

When the 80486 microprocessor is in 32-bit mode and branches to an address, it always reads in four double words. It reads these double words in four separate bus transactions. If the microprocessor does not use all four double words, the inverse assembler marks the unused words as prefetch.

The 80486 microprocessor does not always fetch the four doublewords from consecutive addresses. If the branch is to an address with the least significant nibble of the address equal to 0, 1, 2, or 3, the 80486 will read in the first double word starting at byte 0, then the next three double words starting from bytes 4, 8, and C. However, if the branch is to an address with the least significant nibble of the address equal to 4, 5, 6, or 7, the 80486 will read in the first double word starting at byte 4, then a double word starting from byte 0, then a double word from byte C, and finally a double word from byte 8. Once the 80486 fetches the first four double words, it will fetch all subsequent code from consecutive addresses until the next branch.

To deal with this microprocessor phenomenon, the inverse assembler displays the information in the order in which the opcodes are executed. It also reconstructs the least significant nibbles of the the opcode addresses, and displays those nibbles on the left side of the opcode.

The ADDR label displays addresses in the actual order they are fetched by the microprocessor.

Unused Code Read

Some states are marked as "unused code read." This occurs when the last hexadecimal digit of the address for that state is less than the last hexadecimal digit of the first address that execution transferred to within that prefetched line. For example, execution transfers to an address that ends in the hexadecimal digit 8, the states fetched from addresses 0 and 4 are displayed with the status "unused code read."

E7A8	Execution transfers to address whose last hexadecimal digit is 8.
E7AC	
E7A0	State is marked "unused code read" since last digit is less than 8.
E7A4	State is marked "unused code read" since last digit is less than 8.
E7B0	Start of new prefetch line

Some states are marked as "code read." This occurs when all four bytes of the state were used to decode the instruction of the previous state.

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request Displayed if the microprocessor is asked to perform a task which it cannot do.

Fatal Data Error Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Invalid Status Displayed if the status field for the current state is not valid.

Illegal Opcode Displayed if the inverse assembler encounters an illegal 80486 instruction.

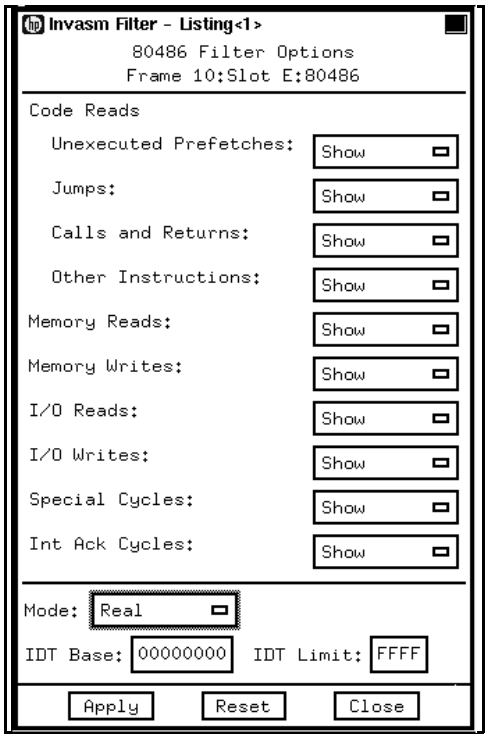
Reserved Opcode Displayed if the inverse assembler encounters a reserved coprocessor instruction.

No Operand Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause. Asterisks (*) are used to indicate missing operands.

The IA486E inverse assembler

The IA486E inverse assembler contains all the functions of the IA486 inverse assembler (see previous sections), plus additional features. For the enhanced inverse assembler, the logic analyzer must meet the software version requirements listed in "Logic analyzer software version requirements" on page 1-5.

The Invasm menu contains four functions: Load (HP 16600/700 only), Filtering (see figure below), Align, and Options. The following sections describe these functions.



Filter Menu

Load

The Load function lets you load a different inverse assembler and apply it to the data in the Listing menu. In some cases you may have acquired raw data; you can use the Load function to apply an inverse assembler to that data.

Filter

The Filter function brings up a Show/Suppress menu, Mode, and IDT description entry. You can change the Show/Suppress settings to specify whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The previous figure shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. The previous figure shows the settings to suppress unexecuted prefetches. The figure on page 3-14 shows a listing with the unexecuted prefetches suppressed, so that only executed instructions are displayed. A comparison of this figure with the figure on page 3-13 shows the difference in the listing display.

Second, particular operations can be isolated by suppressing all other operations. For example, I/O operations can be shown, with all other operations suppressed, allowing quick analysis of I/O operations.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

IDT Description

The IDT Description settings include Mode, IDT Start, and IDT Size. Mode can be Protected, Real, or Virtual. IDT Start refers to the starting address of the Interrupt Descriptor Table, and IDT Size refers to the size of the table. Set these functions to match the target system settings.

In most cases, the inverse assembler can automatically determine the target system settings, and will operate properly regardless of the settings entered. The inverse assembler uses the information from these settings only in cases of uncertainty. If you suspect that the inverse assembler is disassembling improperly, check that these settings match your target system.

Align

Align enables the inverse assembler to re-align with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To align the inverse assembler, use the procedure described earlier.

Options

The Options menu lets you change the width of the display.

Coprocessor Support

Numeric coprocessor support is built into the 80486 microprocessor. The inverse assemblers decode the instructions for the floating point unit.

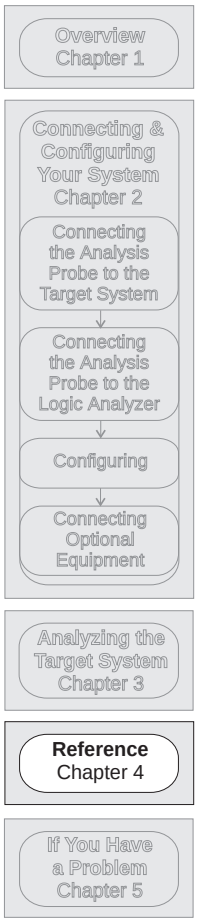
Reference

Reference

This chapter contains additional reference information including the signal mapping for the HP E2411C Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics of the analysis probe
- Operating characteristics of the probe adapters
- Operating characteristics of the debug port
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts



Operating characteristics of the analysis probe

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe. These characteristics are included as additional information for the user.

Operating Characteristics of the Analysis Probe

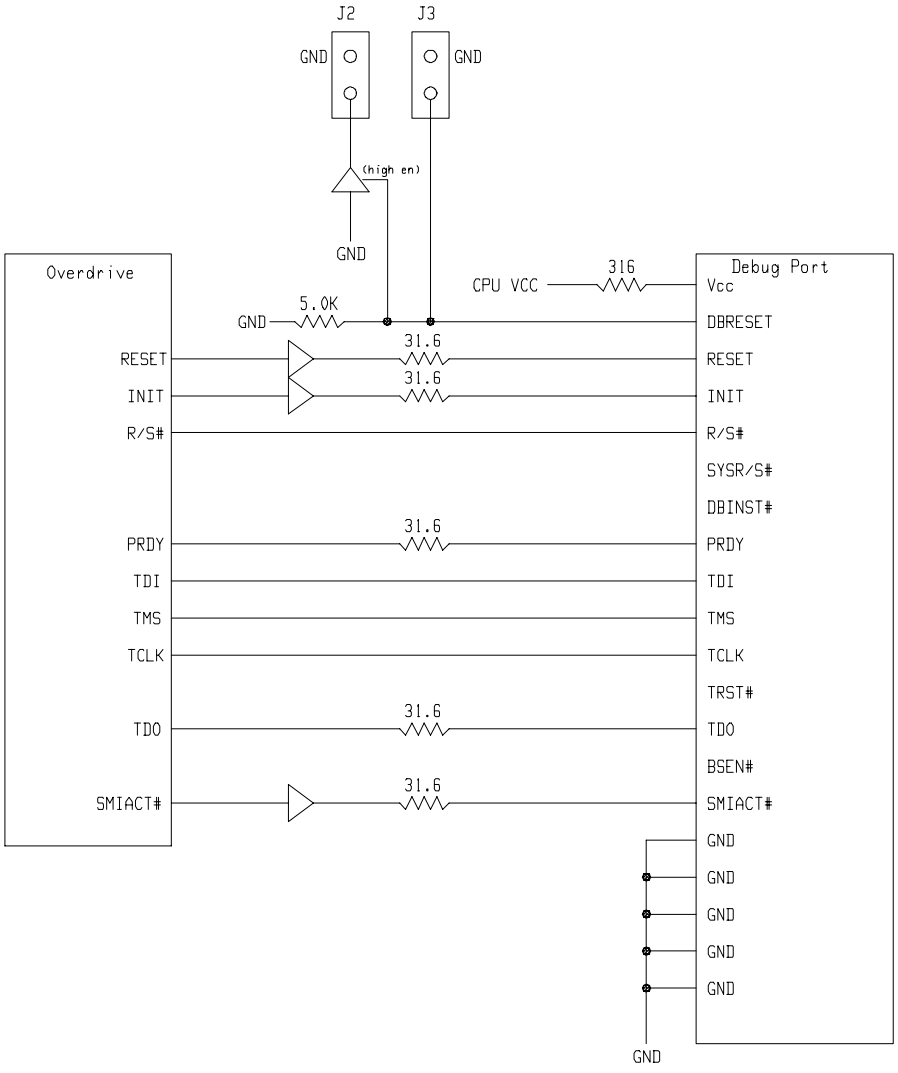
Microprocessor Compatibility	Intel 80486DX/DX2/DX4/Overdrive, 80486SX/SL, and 80487SX microprocessors, and all microprocessors made by other manufacturers that comply with Intel 80486DX and 80486/7SX/SL specifications.
Microprocessor Package	168-pin PGA 80486DX/DX2 169-pin PGA 80487SX 236, 237, 238, 239-pin PGA 80486 Overdrive 208-pin PQFP 176-pin TQFP
Accessories Required	HP E5344A for use with 208-pin PQFP (Option 003) HP E5353A for use with 176-pin TQFP (Option 004)
Maximum Speed	50 MHz bus speed
Power Requirements	1A maximum @ 5V, supplied by the logic analyzer. CAT I, Pollution degree 2.
Logic Analyzer Required	HP 1660A/AS/C/CS/CP, HP 1661A/AS/C/CS/CP, HP 1670A/D, HP 1671A/D, HP 16550A (one or two cards), HP 16554A/55A/56A (two cards), HP 16555D/56D (two cards), HP 16600A, HP 16601A, HP 16602A
Logic Analyzer Software Version Required	See chapter 1
Number of Probes Required	Six 16-channel probes are required for inverse assembly. One additional connector provides additional status signals.

Operating Characteristics of the Analysis Probe (Continued)

Signal Line Loading	A31 - A2, BREQ, D/C#, D31 - D0, FLUSH#, HOLD, INTR, LOCK#, M/IO#, PCD, PLOCK#, PWT, RESET, W/R# CACHE#, BLEN#, HITM#, HIT#, UP#, INV, R/S#, PRDY NMI, INIT, IGNNE#, FERR#, ETRDY#, ETADS, SMIACT# SMI#, PCHK#, EWBE, WB/WT#		1 FCT load
	CLK		4.5 pF
	BS8#, BS16#, BOFF#, HLDA, KEN#		8.5 pF (bipolar PAL input)
	ADS#, BRDY#, RDY#, BE3# - BE0#, BLAST#, EADS# AHOLD		1 FCT load + 1 bipolar PAL input
	BRDYC#		1 FCT load + 1 bipolar PAL input + 10 kOhm pull-up to +5 V
Environmental Temperature	Operating	0 to 55 degrees C (+32 to +131 degrees F)	
	Non operating	-40 to +75 degrees C (-40 to +167 degrees F)	
Altitude	Operating	4,600 m (15,000 ft)	
	Non operating	15,300 m (50,000 ft)	
Humidity	Up to 90% non condensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.		

Operating characteristics of the debug port

The following diagram shows the signals and logic used to implement the debug port on the HP E2411C Analysis Probe. This debug port can be used with the Intel debugger.



Debug Port to be Used With the Intel Debugger

Theory of operation and clocking

The figure on the following page shows the block diagram of the analysis probe.

Latching signals and clocking the logic analyzer is a two-step process. The analysis probe latches the address bus, data bus, and status and control information into the active buffers on the rising CPU CLK edge. The rising CPU CLK also clocks a state machine in the analysis probe, which drives the J clock of the logic analyzer. Setting the logic analyzer to trigger on the rising edge of JCLK will cause the logic analyzer to capture a state for every microprocessor clock.

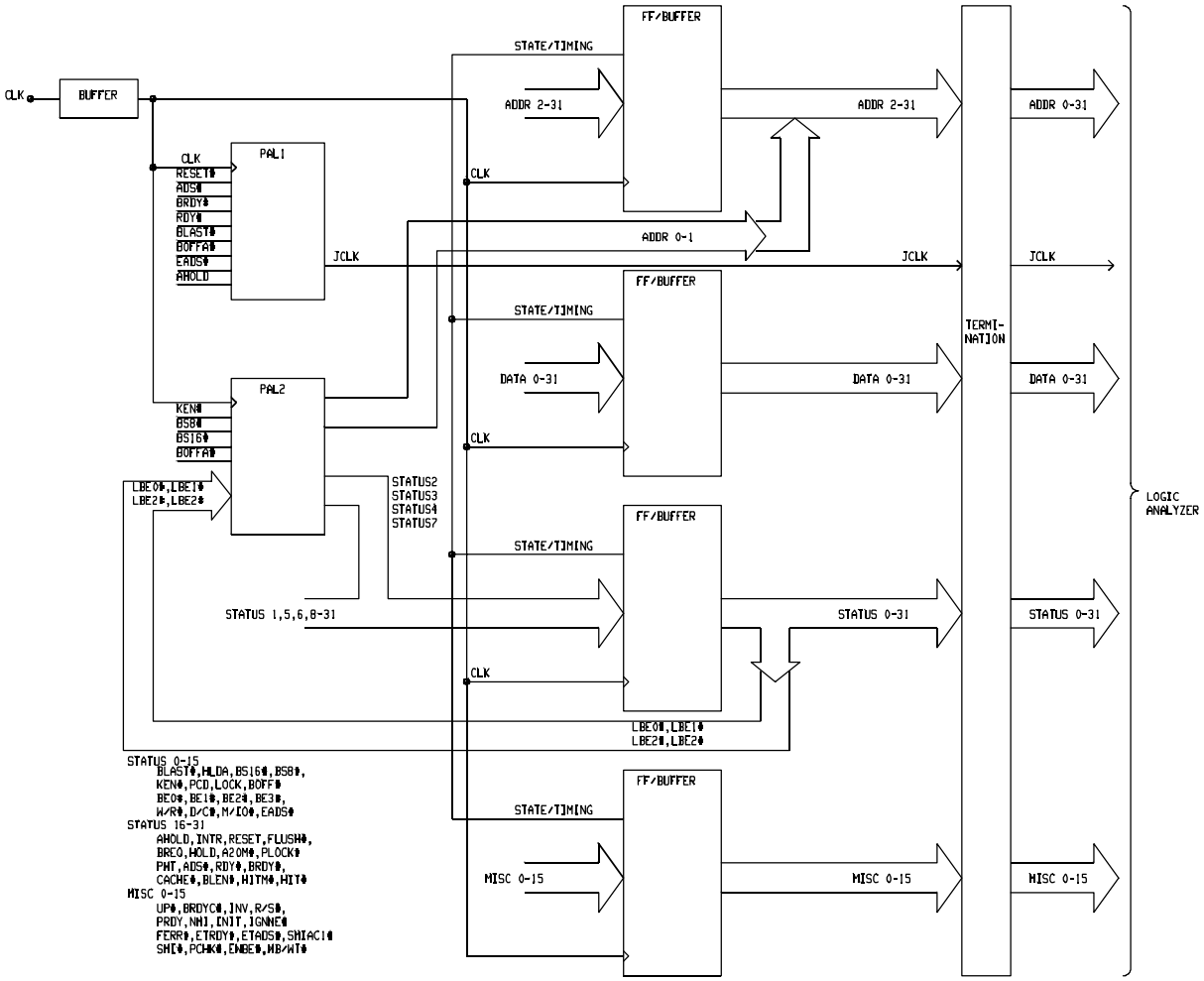
Once the CLK signal is high, the qualifier generator PAL examines the state of the cycle, the current control signals, and the clock qualification switches. If the sample is valid (according to the above parameters), the PAL drives the qualifier KCLK high. If the sample is not valid, the PAL holds the qualifier low. The next sample is then latched into the analysis probe on the next CLK rising edge. Setting the logic analyzer to capture on the rising edge of JCLK with the KCLK qualifier high provides State-per-transfer mode.

The KEN#, BS8#, and BS16# signals are always held one additional state, so that they are aligned with the proper cycle for RDY#, BRDY#, and the data bus.

The "No CI sample" switch controls an address clock enable (a_clk_en) signal. If "Cache inval smpl" is selected, a_clk_en prevents the logic analyzer from sampling whenever AHOLD is high. ADDR is continuously sampled on every rising edge of CLK regardless of the Cache inval (CI) switch setting.

The byte enable signals (BE0# - BE3#) are sampled with the status signals. They also generate address bits A0 and A1, which mimics the internal operation of the microprocessor.

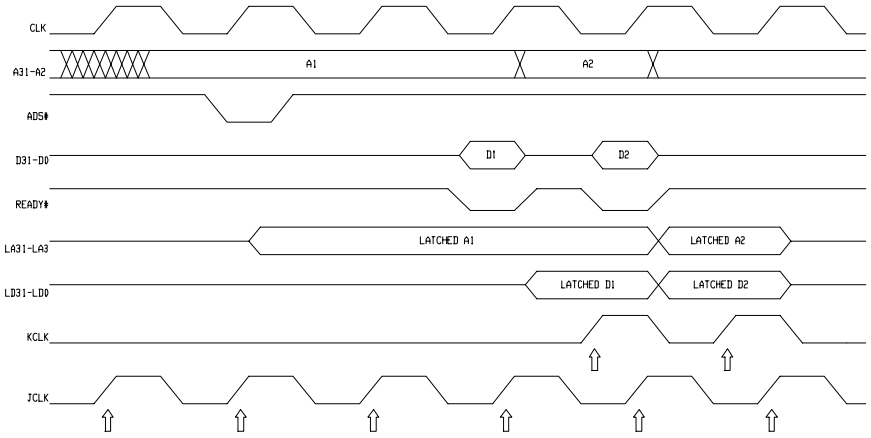
The CLK signal from the microprocessor is routed to a phase-lock loop/buffer. The phase-lock loop provides the small propagation delay required for high-speed operation. The speed-selection switch on the analysis probe allows the phase-lock loop to continue operating within specification during low-speed operation.



Block Diagram

Timing

In Timing mode, the latches on the analysis probe act like flow through buffers. The signals from the microprocessor go directly from the target system to the logic analyzer, with a one ns channel-to-channel skew. However, signals KEN#, BS8#, BS16#, and BOFF# are delayed by one clock. The illustration below shows a timing diagram.



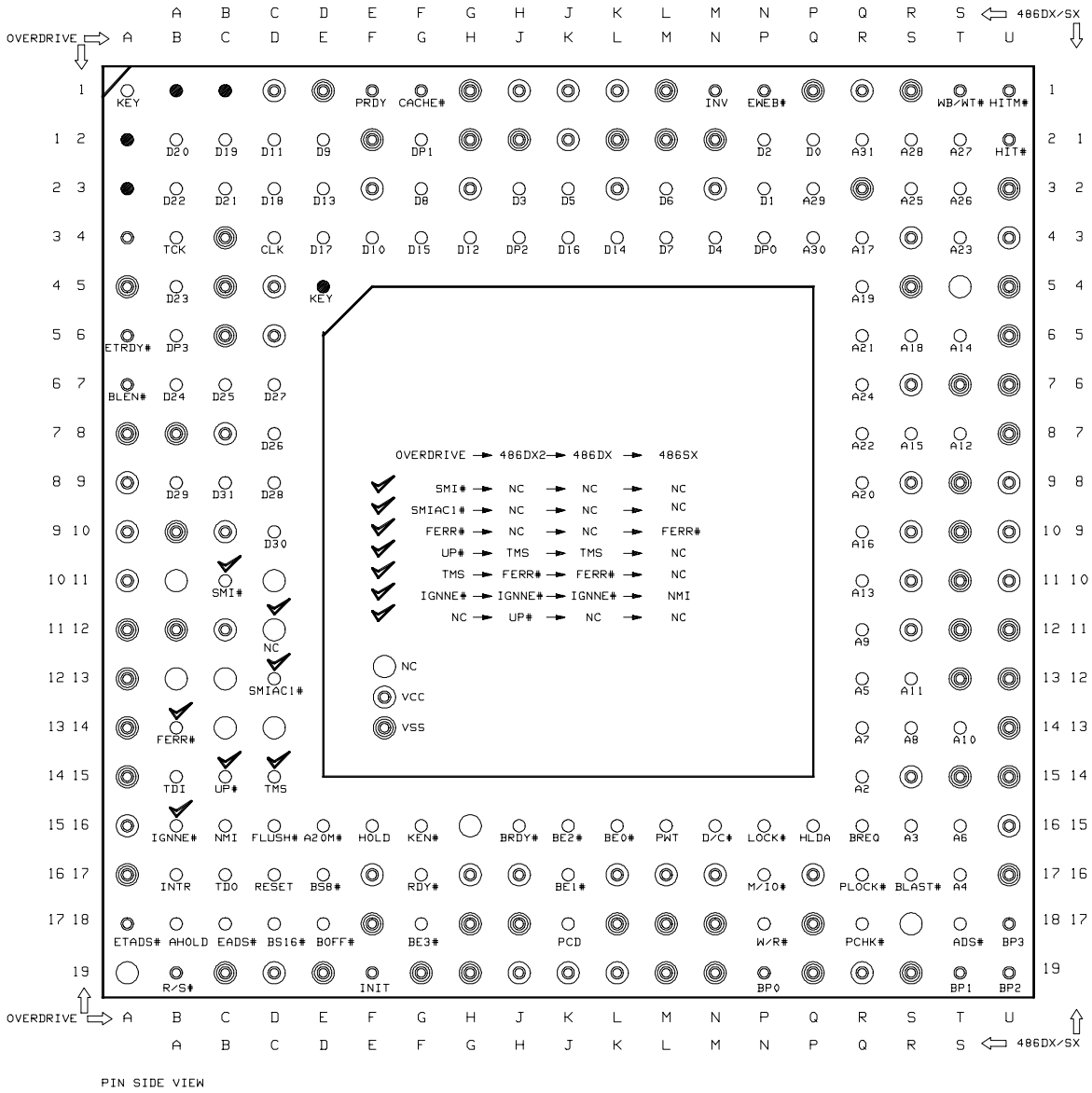
Timing Diagram

Signal-to-connector mapping

The following figures show the analysis probe socket diagram and pin numbers for the PQFP and TQFP adapters. The table after the diagrams lists the electrical interconnections implemented with the analysis probe.

Analysis Probe PGA Socket Diagram

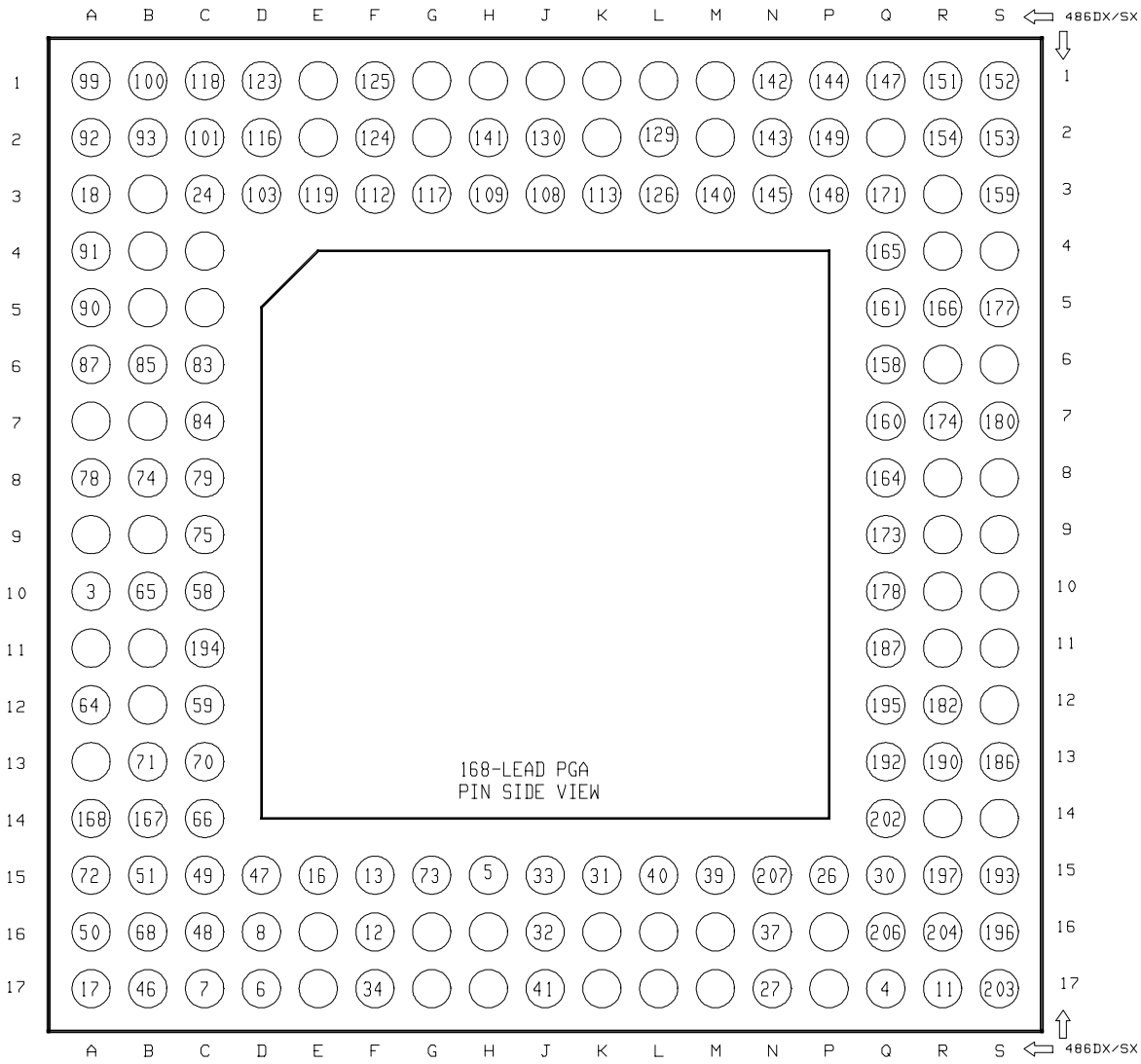
The following illustration shows the analysis probe PGA socket diagram.



Analysis Probe PGA Socket Signal Names

208-pin PQFP to 168-pin PGA adapter

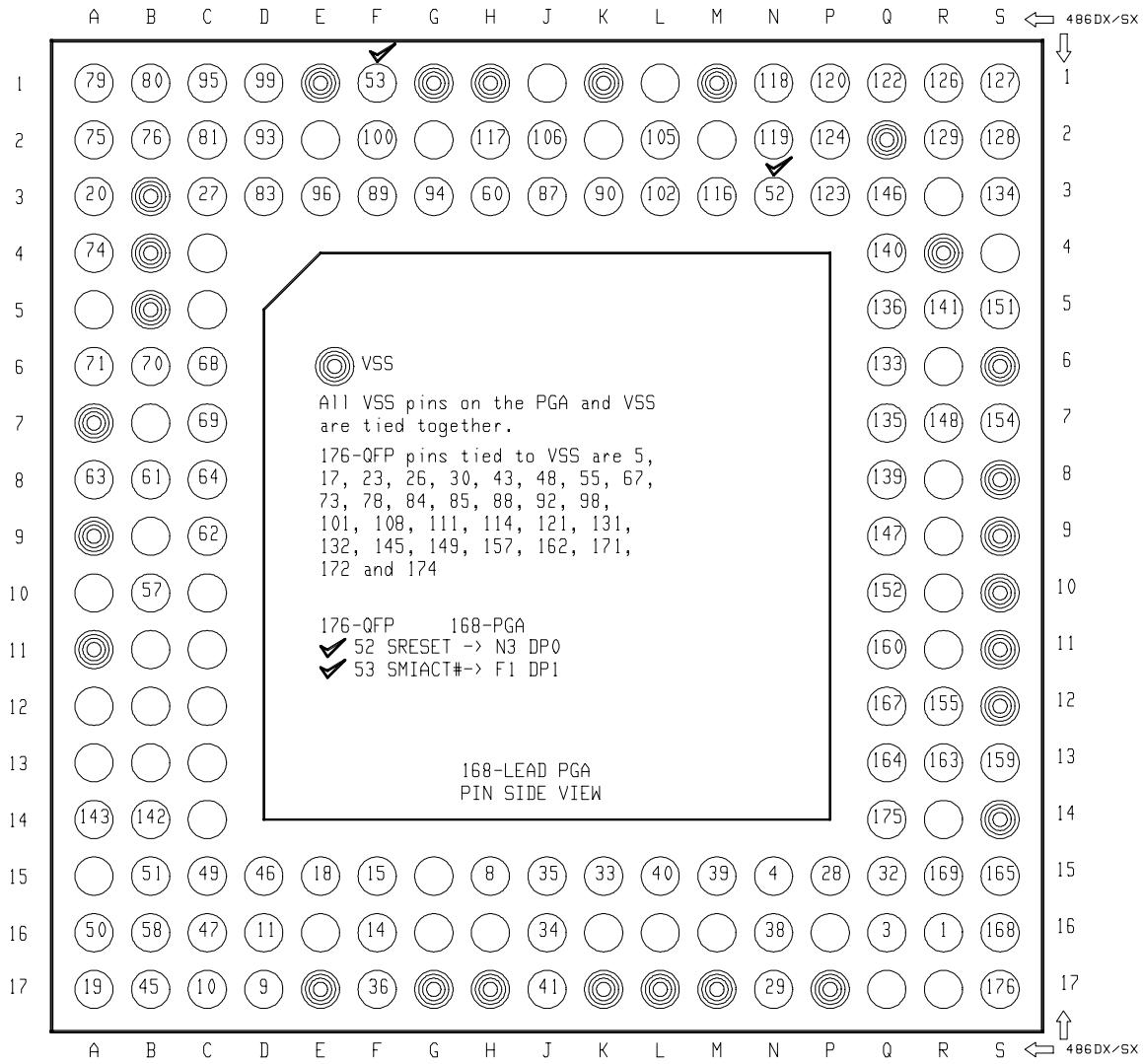
The following illustration shows the 168-pin PGA mapping for the 208-pin PQFP adapter board. The pin names on the 168-pin PGA are the same as those shown on the analysis probe socket diagram.



208-pin PQFP Transition Board Mapping

176-pin TQFP to 168-pin PGA adapter

The following illustration shows the 168-pin PGA mapping for the 176-pin TQFP transition board. The pin names on the 168-pin PGA are the same as those shown on the analysis probe socket diagram.



176-pin TQFP Transition Board Mapping

This table lists the signal-to-connector mapping for the HP E2411C analysis probe.

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
1	clk1	D4	C3	CLK	--
1	clk2	--	--	--	clock qualifier
1	0	S17	R16	BLAST#	BLAST
1	1	Q16	P15	HLDA	HLDA
1	2	D18	C17 *	DBS16#	SIZE
1	3	E17	D16 *	DBS8#	SIZE
1	4	G16	F15 *	DKEN#	KEN
1	5	K18	J17	PCD	PCD
1	6	P16	N15	LOCK#	LOCK
1	7	E18	D17 *	BOFFA#	BOFFA
1	8	L16	K15	BE0#	BE
1	9	K17	J16	BE1#	BE
1	10	K16	J15	BE2#	BE
1	11	G18	F17	BE3#	BE
1	12	P18	N17	W/R#	CYCLE
1	13	N16	M15	D/C#	CYCLE
1	14	P17	N16	M/IO#	CYCLE
1	15	C18	B17	EADS#	EADS

* Delayed versions of the original signals. Each of these signals is delayed by one CLK cycle in Timing mode and State-per-clock mode.

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
2	clk1	--	--	--	clock qualifier
2	0	B18	A17	AHOLD	AHOLD
2	1	B17	A16	INTR	INTR
2	2	D17	C16	RESET	RESET
2	3	D16	C15	FLUSH#	FLUSH
2	4	R16	Q15	BREQ	BREQ
2	5	F16	E15	HOLD	HOLD
2	6	E16	D15	A20M#	A20M
2	7	R17	Q16	PLOCK#	PLOCK
2	8	M16	L15	PWT	PWT
2	9	T18	S17	ADS#	ADS
2	10	G17	F16	RDY#	RDY
2	11	J16	H15	BRDY#	BRDY
2	12	G1	--	CACHE#	CACHE
2	13	A7	--	BLEN#	BLEN
2	14	V1	--	HITM#	HITM
2	15	V2	--	HIT#	HIT

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
3	clk1	D15	C14	TMS	--
3	0	Q2	P1	D0	DATA_L
3	1	P3	N2	D1	DATA_L
3	2	P2	N1	D2	DATA_L
3	3	J3	H2	D3	DATA_L
3	4	N4	M3	D4	DATA_L
3	5	K3	J2	D5	DATA_L
3	6	M3	L2	D6	DATA_L
3	7	M4	L3	D7	DATA_L
3	8	G3	F2	D8	DATA_L
3	9	E2	D1	D9	DATA_L
3	10	F4	E3	D10	DATA_L
3	11	D2	C1	D11	DATA_L
3	12	H4	G3	D12	DATA_L
3	13	E3	D2	D13	DATA_L
3	14	L4	K3	D14	DATA_L
3	15	G4	F3	D15	DATA_L

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
4	clk1	B15	A14	TDI	--
4	0	K4	J3	D16	DATA_H
4	1	E4	D3	D17	DATA_H
4	2	D3	C2	D18	DATA_H
4	3	C2	B1	D19	DATA_H
4	4	B2	A1	D20	DATA_H
4	5	C3	B2	D21	DATA_H
4	6	B3	A2	D22	DATA_H
4	7	B5	A4	D23	DATA_H
4	8	B7	A6	D24	DATA_H
4	9	C7	B6	D25	DATA_H
4	10	D8	C7	D26	DATA_H
4	11	D7	C6	D27	DATA_H
4	12	D9	C8	D28	DATA_H
4	13	B9	A8	D29	DATA_H
4	14	D10	C9	D30	DATA_H
4	15	C9	B8	D31	DATA_H

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
5	clk1	C17	B16	TDO	--
5	0	--	--	A0	ADDR_L
5	1	--	--	A1	ADDR_L
5	2	R15	Q14	A2	ADDR_L
5	3	S16	R15	A3	ADDR_L
5	4	T17	S16	A4	ADDR_L
5	5	R13	Q12	A5	ADDR_L
5	6	T16	S15	A6	ADDR_L
5	7	R14	Q13	A7	ADDR_L
5	8	S14	R13	A8	ADDR_L
5	9	R12	Q11	A9	ADDR_L
5	10	T14	S13	A10	ADDR_L
5	11	S13	R12	A11	ADDR_L
5	12	T8	S7	A12	ADDR_L
5	13	R11	Q10	A13	ADDR_L
5	14	T6	S5	A14	ADDR_L
5	15	S8	R7	A15	ADDR_L

80486 Signal List

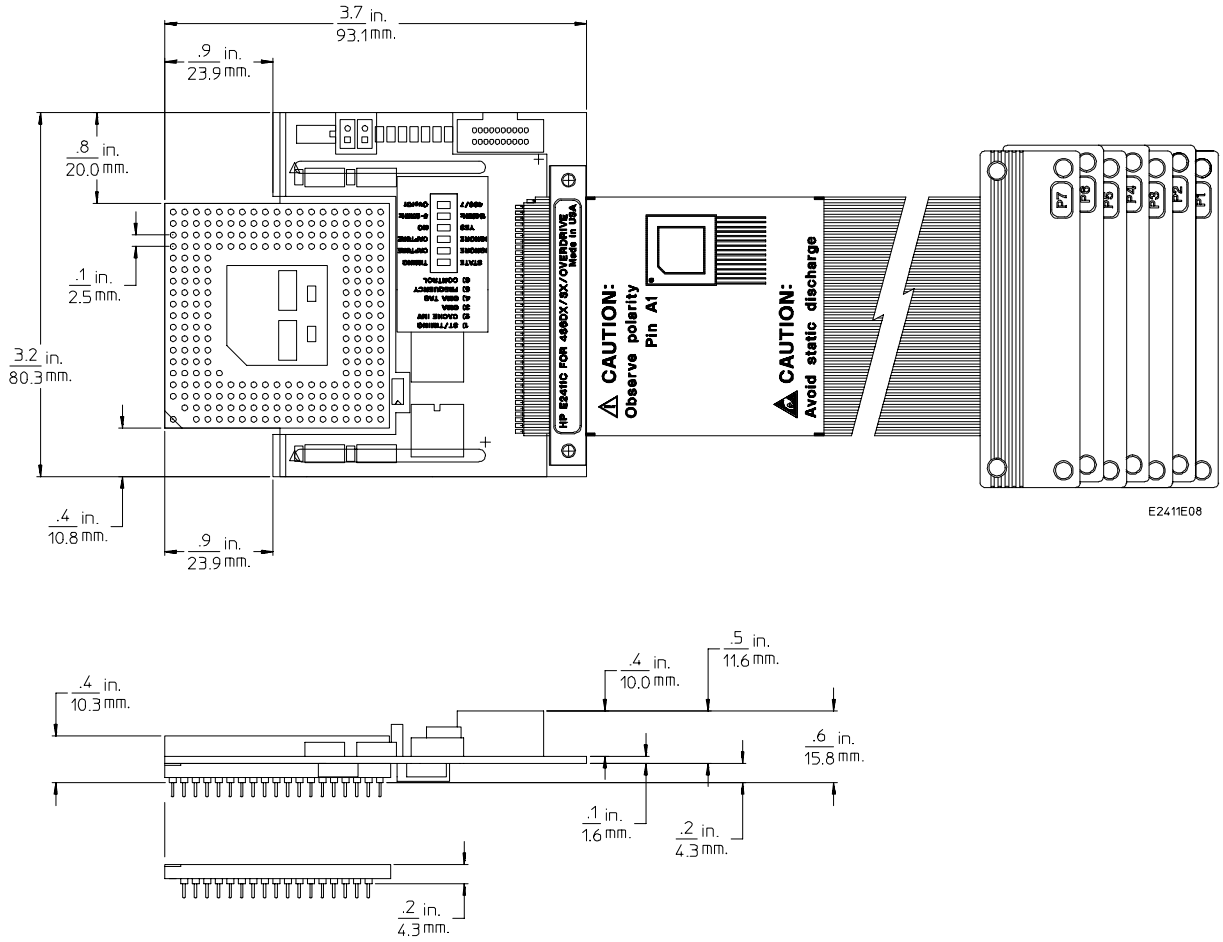
HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
6	clk1	D4	C3	CLK	--
6	0	R10	Q9	A16	ADDR_H
6	1	R4	Q3	A17	ADDR_H
6	2	S6	R5	A18	ADDR_H
6	3	R5	Q4	A19	ADDR_H
6	4	R9	Q8	A20	ADDR_H
6	5	R6	Q5	A21	ADDR_H
6	6	R8	Q7	A22	ADDR_H
6	7	T4	S3	A23	ADDR_H
6	8	R7	Q6	A24	ADDR_H
6	9	S3	R2	A25	ADDR_H
6	10	T3	S2	A26	ADDR_H
6	11	T2	S1	A27	ADDR_H
6	12	S2	R1	A28	ADDR_H
6	13	Q3	P2	A29	ADDR_H
6	14	Q4	P3	A30	ADDR_H
6	15	R2	Q1	A31	ADDR_H

80486 Signal List

HP E2411C Pod	Analyzer Probe	Overdrive Pin	80486 Pin	Pin Mnemonic	Label
7	clk1	--	--	--	clock qualifier
7	0	C15	B14	UP#	MISC0
7	1	T5	S4	BRDYC#	MISC1
7	2	N1	--	INV	MISC2
7	3	B19	A18	R/S#	MISC3
7	4	F1	--	PRDY	MISC4
7	5	C16	B15	NMI	MISC5
7	6	F19	E18	INIT	MISC6
7	7	B16	A15	IGNNE#	MISC7
7	8	B14	A13	FERR#	MISC8
7	9	A6	--	ETRDY#	MISC9
7	10	A18	--	ETADS#	MISC10
7	11	D13	C12	SMIAC#	MISC11
7	12	C11	D10	SMI#	MISC12
7	13	R18	Q17	PCHK#	MISC13
7	14	P1	--	EWBE#	MISC14
7	15	T1	--	WB/WT#	MISC15

Circuit board dimensions

The figure below lists the dimensions for the analysis probe circuit board. The dimensions are listed in inches and millimeters.



Analysis Probe Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

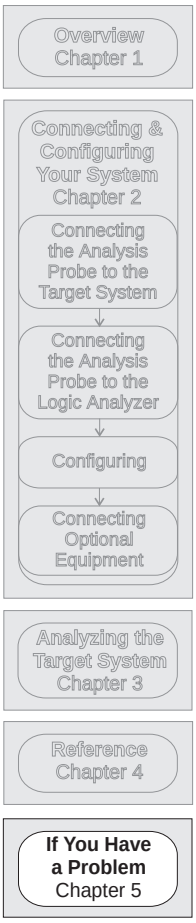
Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

HP Part Number	Description
HP E2411C	
E2411-69504	Exchange Circuit Assembly
E2411-66504	Circuit Board Assembly
E2411-68705	Inverse Assembler Disk Pouch
1200-1790	Pin Protector IC Socket (168-pin 80486 footprint)
1200-1789	Pin Protector IC Socket (238-pin 80486DX2 Overdrive footprint)
Locator Base Solution for 208-pin PQFP packages	
E5318A	Probe Adapter
E5344A	80486 Adapter Board
HP E5353A Elastomeric Probing System for 176-pin TQFP packages	
E5352A	Transition Board
E5348A	Probe Adapter
E5350A	Flex Adapter

If You Have a Problem

If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Hewlett-Packard Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the analysis probe and target system.**

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.**

- ☐ **Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See "Capacitive Loading" in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the HP 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the HP 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the HP 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

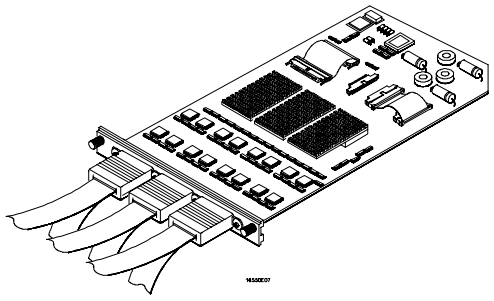
For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

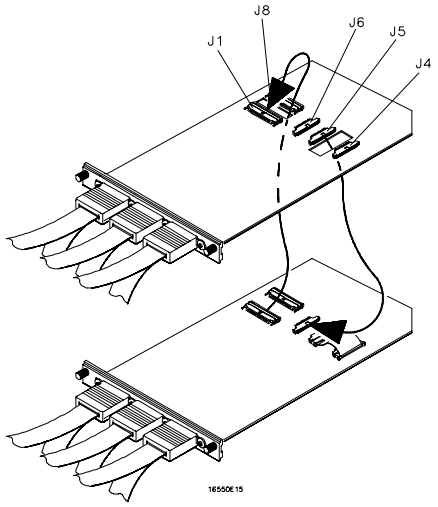
This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card HP 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations

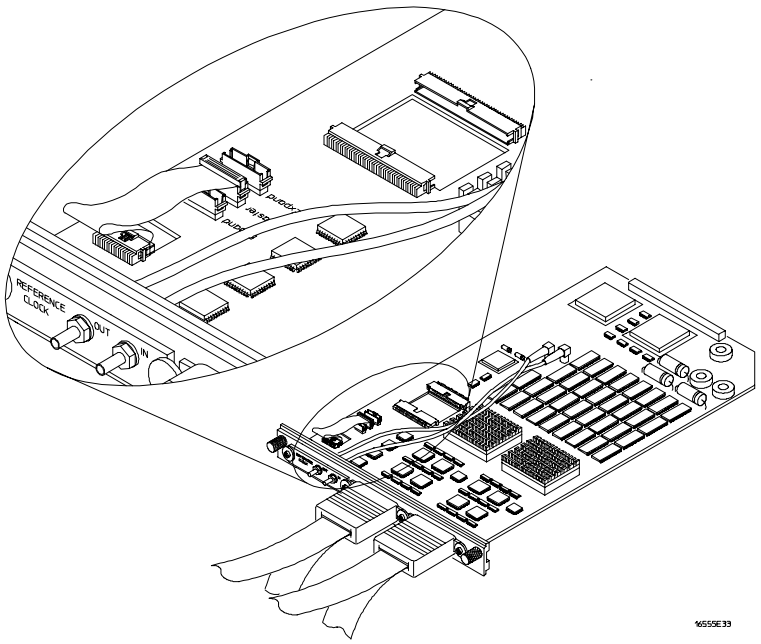


Cable Connections for Two-Card HP 16550A Installations

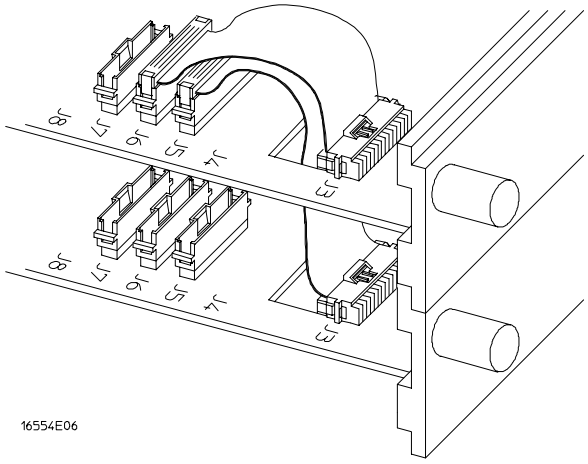
See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

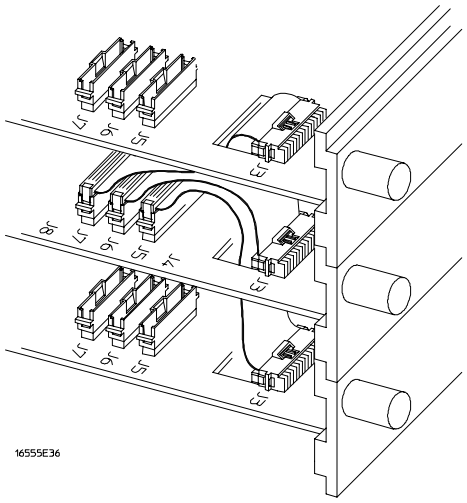
The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on HP 16554A, HP 16555A/D, and HP 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16554/55/56 Installations



Cable Connections for Two-Card HP 16554/55/56 Installations



Cable Connections for Three-Card HP 16554/55/56 Installations

See Also

The HP 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an HP 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The HP 16505A prototype analyzer acts as an analysis and display processor for the HP 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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About this edition

This is the *HP E2411C Analysis Probe for Intel 80486DX/2/4/Overdrive, 80486SX/SL, and 80487SX User's Guide*.

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.